PHILIPS

Data handbook

Electronic
components
and materials

Semiconductors

Book S5 1984

Field-effect transistors

FIELD-EFFECT TRANSISTORS

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DATA HANDBOOK SYSTEM

Our Data Handbook System comprises more than 50 books with specifications on electronic components, subassemblies and materials. It is made up of four series of handbooks:

ELECTRON TUBES	BLUE
SEMICONDUCTORS	RED
INTEGRATED CIRCUITS	PURPLE
COMPONENTS AND MATERIALS	GREEN

The contents of each series are listed on pages iv to viii.

The data handbooks contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

When ratings or specifications differ from those published in the preceding edition they are indicated with arrows in the page margin. Where application information is given it is advisory and does not form part of the product specification.

Condensed data on the preferred products of Philips Electronic Components and Materials Division is given in our Preferred Type Range catalogue (issued annually).

Information on current Data Handbooks and on how to obtain a subscription for future issues is available from any of the Organizations listed on the back cover.
Product specialists are at your service and enquiries will be answered promptly.

ELECTRON TUBES (BLUE SERIES)

The blue series of data handbooks is comprised of the following parts:

T1	**Tubes for r.f. heating**
T2a	**Transmitting tubes for communications, glass types**
T2b	**Transmitting tubes for communications, ceramic types**
T3	**Klystrons, travelling-wave tubes, microwave diodes**
ET3	**Special Quality tubes, miscellaneous devices** (will not be reprinted)
T4	**Magnetrons**
T5	**Cathode-ray tubes** Instrument tubes, monitor and display tubes, C.R. tubes for special applications
T6	**Geiger-Müller tubes**
T7	**Gas-filled tubes** Segment indicator tubes, indicator tubes, dry reed contact units, thyratrons, industrial rectifying tubes, ignitrons, high-voltage rectifying tubes, associated accessories
T8	**Picture tubes and components** Colour TV picture tubes, black and white TV picture tubes, colour monitor tubes for data graphic display, monochrome monitor tubes for data graphic display, components for colour television, components for black and white television and monochrome data graphic display
T9	**Photo and electron multipliers** Photomultiplier tubes, phototubes, single channel electron multipliers, channel electron multiplier plates
T10	**Camera tubes and accessories**
T11	**Microwave semiconductors and components**
T12	**Vidicons and Newvicons**
T13	**Image intensifiers**
T14	**Infrared detectors**

SEMICONDUCTORS (RED SERIES)

The red series of data handbooks comprises:

S1	**Diodes** Small-signal germanium diodes, small-signal silicon diodes, voltage regulator diodes(< 1,5 W), voltage reference diodes, tuner diodes, rectifier diodes
S2	**Power diodes, thyristors, triacs** Rectifier diodes, voltage regulator diodes (> 1,5 W), rectifier stacks, thyristors, triacs
S3	**Small-signal transistors**
S4a	**Low-frequency power transistors and hybrid modules**
S4b	**High-voltage and switching power transistors**
S5	**Field-effect transistors**
S6	**R.F. power transistors and modules**
S7	**Microminiature semiconductors for hybrid circuits**
S8	**Devices for optoelectronics** Photosensitive diodes and transistors, light-emitting diodes, displays, photocouplers, infrared sensitive devices, photoconductive devices.
S9	**Power MOS transistors**
S10	**Wideband transistors and wideband hybrid IC modules**

INTEGRATED CIRCUITS (PURPLE SERIES)

The purple series of data handbooks comprises:

EXISTING SERIES

IC1	**Bipolar ICs for radio and audio equipment**
IC2	**Bipolar ICs for video equipment**
IC3	**ICs for digital systems in radio, audio and video equipment**
IC4	**Digital integrated circuits** CMOS HE4000B family
IC5	**Digital integrated circuits – ECL** ECL10 000 (GX family), ECL100 000 (HX family), dedicated designs
IC6	**Professional analogue integrated circuits**
IC7	**Signetics bipolar memories**
IC8	**Signetics analogue circuits**
IC9	**Signetics TTL logic**
IC10	**Signetics Integrated Fuse Logic (IFL)**
IC11	**Microprocessors, microcomputers and peripheral circuitry**

NEW SERIES

IC01N	**Radio, audio and associated systems** Bipolar, MOS	
IC02N	**Video and associated systems** Bipolar, MOS	
IC03N	**Telephony equipment** Bipolar, MOS	
IC04N	**HE4000B logic family** CMOS	
IC05N	**HE4000B logic family uncased integrated circuits** CMOS	(published 1984)
IC06N	**PC54/74HC/HCU/HCT logic families** HCMOS	
IC07N	**PC54/74HC/HCU/HCT uncased integrated circuits** HCMOS	
IC08N	**10K and 100K logic family** ECL	
IC09N	**54/74: STD, LS, S, F logic series** TTL	
IC10N	**Memories** MOS, TTL, ECL	
IC11N	**Analogue - industrial**	
IC12N	**Semi-custom gate arrays & cell libraries** ISL, ECL, CMOS	
IC13N	**Semi-custom integrated fuse logic** IFL series 20/24/28	
IC14N	**Microprocessors, microcontrollers & peripherals** Bipolar, MOS	

Note

Books available in the new series are shown with their date of publication.

COMPONENTS AND MATERIALS (GREEN SERIES)

The green series of data handbooks comprises:

C1	**Assemblies for industrial use** PLC modules, PC20 modules, HNIL FZ/30 series, NORbits 60-, 61-, 90-series, input devices, hybrid ICs
C2	**Television tuners, video modulators, surface acoustic wave filters**
C3	**Loudspeakers**
C4	**Ferroxcube potcores, square cores and cross cores**
C5	**Ferroxcube for power, audio/video and accelerators**
C6	**Synchronous motors and gearboxes**
C7	**Variable capacitors**
C8	**Variable mains transformers**
C9	**Piezoelectric quartz devices** Quartz crystal units, temperature compensated crystal oscillators, compact integrated oscillators, quartz crystal cuts for temperature measurements
C10	**Connectors**
C11	**Non-linear resistors** Voltage dependent resistors (VDR), light dependent resistors (LDR), negative temperature coefficient thermistors (NTC), positive temperature coefficient thermistors (PTC)
C12	**Variable resistors and test switches**
C13	**Fixed resistors**
C14	**Electrolytic and solid capacitors**
C15	**Film capacitors, ceramic capacitors**
C16	**Permanent magnet materials**
C17	**Stepping motors and associated electronics**
C18	**D.C. motors**
C19	**Piezoelectric ceramics**
C20	**Wire-wound components**

N-channel junction field-effect transistors

type number	envelope	RATINGS			CHARACTERISTICS							remarks
		$\pm V_{DS}$ V	P_{tot} at T_{amb} mW	°C	$-I_{GSS}$ max. nA	I_{DSS} min.-max. mA	$-V_{(P)GS}$ max. V	$\lvert y_{fs}\rvert$ min. f = 1 kHz mA/V	C_{rs} typ. pF	F typ. dB	V_n max. µV	
BC264A	TO-92 var.	30	300	25	10	2,0-4,5	> 0,5	2,5	1,2	0,5	—	hi-fi amplifiers and a.f. equipment
BC264B						3,5-6,5		3,0				
BC264C						5,0-8,0		3,5				
BC264D						7,0-12,0		4,0				
BF245A	TO-92 var.	30	300	75	5	2,0-6,5	8,0	3,0-6,5	1,1	1,5	—	d.c., l.f. and h.f. amp.
BF245B						6-15						
BF245C						12-25						
BF247A	TO-92	25	250	75	5	30-80	0,6-14,5	8	3,5	—	—	v.h.f. and u.h.f. amp. general purpose sw.
BF247B						60-140						
BF247C						110-250						
BF256A	TO-92 var.	30	300	75	5	3-7	—	4,5	0,7	7,5	—	v.h.f. and u.h.f. appl.
BF256B						6-13						
BF256C						11-18						
BF410A	TO-92 var.	20*	300	75	10	0,7-3,0	typ. 0,8	2,5	0,3	1,5	—	r.f. stages f.m. portables
BF410B						2,5-7,0	typ. 1,5	4,0				r.f. stages car radios
BF410C						6-12	typ. 2,2	6,0				r.f. stages mains radios
BF410D						10-18	typ. 3,0	7,0				mixer stages
BF510	SOT-23	20	250	65	10	0,7-3,0	typ. 0,8	2,5	0,3	1,5	—	r.f. stages f.m. portables
BF511						2,5-7,0	typ. 1,5	4,0				r.f. stages car radios
BF512						6-12	typ. 2,2	6,0				r.f. stages mains radios
BF513						10-18	typ. 3,0	7,0				mixer stages
BFR30	SOT-23	25	250	65	0,2	4-10	5	1,0-4,0	< 1,5	—	0,5	low-level general purpose amplifiers
BFR31						1-5	2,5	1,5-4,5				
BFR101A	SOT-143	30	200	60	5	0,2-1,5	1,0	1,2	—	—	—	source follower
BFR101B						1-5	2,5	2,5	—	—	—	

* Asymmetrical.

N-channel junction field-effect transistors

type number	envelope	RATINGS			CHARACTERISTICS							remarks
		± V_{DS} V	P_{tot} at T_{amb} mW	°C	$-I_{GSS}$ max. nA	I_{DSS} min.-max. mA	$-V_{(P)GS}$ max. V	$\lvert y_{fs} \rvert$ min. f = 1 kHz mA/V	C_{rs} typ. pF	F typ. dB	V_n max. µV	
BFT46	SOT-23	25	250	65	0,2	0,2-1,5	1,2	1,0	< 1,5	–	0,5	general purpose ampl.
BFW10	TO-72	30	300	25	0,1	8-20	8	3,5-6,5	0,6	< 2,5		broad band up to 300 MHz and differential ampl.
BFW11						4-10	6	3,0-6,5				
BFW12	TO-72	30	150	110	0,1	1-5	2,5	2,0	< 0,8	–	0,5	low current-low voltage applications
BFW13						0,2-1,5	1,2	1,0				
BFW61	TO-72	25	300	25	1,0	2-20	8	2,0-6,5	< 2,0	–	–	general purpose ampl.
2N3822	TO-72	50	300	25	0,1	2-10	6	3,0-6,5	< 3,0	< 5	–	general purpose h.f. ampl.
2N3823	TO-72	30	300	25	0,5	4-20	8	3,5-6,5	< 2,0	< 2,5	–	industrial i.f./r.f. ampl.

N-channel junction field-effect transistors for switching

type number	envelope	RATINGS			CHARACTERISTICS						
		$\pm V_{DS}$ V	P_{tot} at T_{amb} mW	°C	$-I_{GSS}$ (I_{SGO}) max. pA	I_{DSS} min. mA	$-V_{(P)GS}$ max. V	$r_{ds\ on}$ max. Ω	C_{rs} max. pF	t_{on} max. ns	t_{off} max. ns
BSR56	SOT-23	40	250	65	1000	50	10	25	5	9	25
BSR57						20	6	40		10	50
BSR58						8	4	60		20	100
BSV78	TO-18	40	350	25	250	50	11	25	5	10	10
BSV79						20	7,0	40		18	16
BSV80						10	5,0	60		30	32
2N3966	TO-72	30	300	25	100	2	6	220	1,5	120	100
2N4091	TO-18	40	1800	25	200	30	10	30	5	25	40
2N4092						15	7,0	50		35	60
2N4093						8	5,0	80		60	80
2N4391	TO-18	40	1800	25	100	50	10	30	3,5	15	20
2N4392						25	5,0	60			35
2N4393						5	3,0	100			50
2N4856	TO-18	40	360	25	250	50	10	25	8	9	25
2N4857		40				20	6	40		10	50
2N4858		40				8	4	60		20	100
2N4859		30				50	10	25		9	25
2N4860		30				20	6	40		10	50
2N4861		30				8	4	60		20	100

N-channel junction field-effect transistors for differential amplifiers

type number	envelope	RATINGS					CHARACTERISTICS							
		individual transistor			total device		individual transistor			total device				
		± V_{DS}	P_{tot} at T_{amb}		P_{tot} at T_{amb}		$-I_{GSS}$	I_{DSS}	$-V_{(P)GS}$	$\lvert \Delta V_{GS} \rvert$	$\left\lvert \frac{d\Delta V_{GS}}{dT} \right\rvert$	$\left\lvert \Delta \frac{1}{g_{fs}} \right\rvert$	$\left\lvert \Delta \frac{g_{os}}{g_{fs}} \right\rvert$	CMRR
			mW	°C	mW	°C	max. pA	mA	max. V	max. mV	max. µV/K	max. Ω	max. µV/V	min. dB
BFQ10	TO-71	30	250	75	250	75	100	0,5-10	3,5	5	5	6	10	100
BFQ11										10	5	6	30	90
BFQ12										10	10	12	30	90
BFQ13										10	20	12	30	90
BFQ14										15	20	12	30	90
BFQ15										20	40	20	30	90
BFQ16										50	50	30	100	80
BFS21	SOT-52	30	300	25	30	100	–	> 1	6	20	75	15	1000	60
BFS21A										10	40	7,5	500	66

Dual-gate N-channel MOS-FETS

type number	envelope	RATINGS				CHARACTERISTICS							remarks
		V_{DB} V_{SB}	V_{DS}	P_{tot} at T_{amb}		$\pm I_{GSS}$ max.	$\pm I_{G1\text{-}SS}$ $\pm I_{G2\text{-}SS}$ max.	I_{DSS}	$-V_{(P)GS}$ $-V_{(P)G1\text{-}S}$	$\lvert y_{fs} \rvert$ f = 1 kHz min.	C_{rs} typ.	F max.	
		V	V	mW	°C	pA	nA	mA	V	mA/V	fF	dB	
BF960*	SOT-103	—	20	225	75	—	50	2-20	< 3,5	9,5	25	2,8**	r.f. stage — UHF TV tuner
BF964*	SOT-103	—	20	225	75	—	50	2-20	< 2,5	15	25	2,8	r.f./mixer stage VHF TV tuner
BF966*	SOT-103	—	20	225	75	—	50	2-20	< 2,5	15	25	3,9	r.f. stage UHF TV tuner
BF980*	SOT-103	—	18	225	75	—	25	—	< 1,3	17	25	2,8**	r.f./mixer stage VHF TV tuner
BF981*	SOT-103	—	20	225	75	—	50	4-25	< 2,5	10	20	2,0	r.f./mixer stage VHF TV tuner
BF982*	SOT-103	—	20	225	75	—	25	—	< 1,3	20	30	1,2**	r.f./mixer stage VHF TV tuner and FM radio tuner
BF989*	SOT-143	—	20	200	60	—	50	2-20	< 2,7	9,5	25	2,8**	u.h.f. — r.f. stage
BF990*	SOT-143	—	18	200	60	—	25	—	< 1,3	17	25	2,8**	u.h.f. — r.f. stage
BF991*	SOT-143	—	20	200	60	—	50	4-25	< 2,5	10	20	2,0	v.h.f. — r.f. stage
BF992*	SOT-143	—	20	200	60	—	25	—	< 1,3	20	30	1,2**	v.h.f. — r.f. stage
BF994*	SOT-143	—	20	200	60	—	50	2-20	< 2,5	15	25	2,8	v.h.f. — r.f. stage
BF996*	SOT-143	—	20	200	60	—	50	2-20	< 2,5	15	25	3,9	u.h.f. — r.f. stage
BFR84*	TO-72	—	20	300	25	—	10	20-55	1,5-3,8	12	30	3,0	general industrial

* Protected against excessive input voltage surges.

** Typical.

N-channel MOS-FET for switching

type number	envelope	RATINGS			CHARACTERISTICS					
		V_{DB} V_{SB} V	P_{tot} at T_{amb} mW	°C	$\pm I_{GSS}$ max. nA	I_{DSX} I_{SDX} max. nA	$r_{ds\ on}$ max. Ω	$r_{DS\ off}$ min. GΩ	C_{rs} max. pF	C_{rd} max. pF
BFR29	TO-72	30	200	25	0,01	–	–	–	0,7	–
BSD10	TO-72	15	275	25	–	–	30	–	0,6	–
BSD12		25								
BSD20	SOT-143	15	230	25	–	–	30	–	0,6	–
BSD22		25								
BSD212	TO-72	15	275	25	–	–	70	–	0,6	–
BSD213		15								
BSD214		25								
BSD215		25								
BSS83	SOT-143	15	230	25	–	–	45	–	0,6	–
BST70A	TO-92 var.		1000	25	100	–	4	–	8	–
BST72A	TO-92 var.		830	25	100	–	10	–	3	–
BST74A	TO-92 var.		1000	25	100	–	12	–	6	–
BST76A	TO-92 var.		1000	25	100	–	10	–	6	–
BST78	TO-126		15 000	25	100	–	15	–	5	–
BSV81	TO-72	30	200	25	0,01	1	100	10	0,5	0,5

In this alphanumeric list we present all n-channel field-effect transistors mentioned in this handbook.

type number	envelope	± V_{DS} max. V	I_{DSS} mA	application	page
BC264A	TO-92 var.	30	2,0 - 4,5	hi-fi amplifiers and a.f. equipment	39
BC264B			3,5 - 6,5		
BC264C			5,0 - 8,0		
BC264D			7,0 - 12,0		
BF245A	TO-92 var.	30	2,0 - 6,5	d.c., l.f. and h.f. amplifiers	45
BF245B			6,0 - 15,0		
BF245C			12 - 25		
BF247A	TO-92 var.	25	30 - 80	v.h.f. and u.h.f. ampl. general purpose switch	57
BF247B			60 - 140		
BF247C			110 - 250		
BF256A	TO-92 var.	30	3 - 7	v.h.f. and u.h.f.	59
BF256B			6 - 13		
BF256C			11 - 18		
BF410A	TO-92 var.	20*	0,7 - 3,0	r.f. stages f.m. portables	71
BF410B			2,5 - 7,0	r.f. stages car radios	
BF410C			6 - 12	r.f. stages mains radios	
BF410D			10 - 18	mixer stages	
BF510	SOT-23	20	0,7 - 3,0	r.f. stage f.m. portables	75
BF511			2,5 - 7,0	r.f. stage car radios	
BF512			6 - 12	r.f. stage mains radios	
BF513			10 - 18	mixer stages	
BF960	SOT-103	20	2 - 20	r.f. stage UHF TV tuner	173
BF964	SOT-103	20	2 - 20	r.f./mixer stage VHF TV tuner	177
BF966	SOT-103	20	2 - 20	r.f. stage UHF TV tuner	181
BF980	SOT-103	18	—	r.f. stage UHF TV tuner	185
BF981	SOT-103	20	4 - 25	r.f./mixer stage VHF TV tuner	189
BF982	SOT-103	20	—	r.f./mixer stage VHF TV tuner and FM radio tuner	197
BF989	SOT-143	20	2 - 20	u.h.f. TV tuners	201
BF990	SOT-143	18	—	u.h.f. TV tuners	203
BF991	SOT-143	20	4 - 25	v.h.f. TV and f.m. tuners	207
BF992	SOT-143	20	—	v.h.f. TV and f.m. tuners	209
BF994	SOT-143	20	2 - 20	u.h.f./v.h.f. TV tuners	211
BF996	SOT-143	20	2 - 20	u.h.f. TV tuners	215
BFQ10	TO-71	30	0,5 - 10	low level differential amplifiers	81
BFQ11					
BFQ12					
BFQ13					
BFQ14					
BFQ15					
BFQ16					
BFR29	TO-72	30**	10 - 40	v.h.f./low leakage/low noise	219

* Asymmetrical.

** V_{DB}.

type number	envelope	± V_{DS} max. V	I_{DSS} mA	application	page
BFR30	SOT-23	25	4 - 10	general purpose amplifiers	89
BFR31			1 - 5		
BFR84	TO-72	20	20 - 55	general industrial	227
BFR101A	SOT-143	30	0,2 - 1,5	source follower	99
BFR101B			1,0 - 5,0		
BFS21	SOT-52	30	> 1	low level differential amplifiers	101
BFS21A					
BFT46	SOT-23	25	0,2 - 1,5	general purpose amplifiers	107
BFW10	TO-72	30	8 - 20	wide-band up to 300 MHz and differential amplifiers	115
BFW11			4 - 10		
BFW12	TO-72	30	1 - 5	low current-low voltage	127
BFW13			0,2 - 1,5		
BFW61	TO-72	25	2 - 20	general purpose	137
BSD10	TO-72	10	–	switch/convertor/chopper	233
BSD12		20			
BSD20	SOT-143	10	–	switch/convertor/chopper	237
BSD22		20	–		
BSD212	TO-72	10	–	switch/convertor/chopper	241
BSD213		10	–		
BSD214		20	–		
BSD215		20	–		
BSR56	SOT-23	40	> 50	switch/chopper	139
BSR57			20 - 100		
BSR58			8 - 80		
BSS83	SOT-143	10	–	switch/switch driver	245
BST70A	TO-92 var.	80	–	high-speed relay and line transformer driver in telephone circuits	249
BST72A	TO-92 var.	80	–		253
BST74A	TO-92 var.	200	–		257
BST76A	TO-92 var.	180	–		261
BST78	TO-202	450	–		265
BSV78	TO-18	40	> 50	switch	143
BSV79			> 20		
BSV80			> 10		
BSV81	TO-72	30*	–	switch/chopper	269
2N3822	TO-72	50	2 - 10	general purpose h.f. ampl.	151
2N3823	TO-72	30	4 - 20	industrial i.f./r.f. ampl.	153
2N3966	TO-72	30	> 2	low power switch	155
2N4091	TO-18	40	> 30	low power switch	159
2N4092			> 15		
2N4093			> 8		

type number	envelope	$\pm V_{DS}$ max. V	I_{DSS} mA	application	page
2N4391	TO-18	40	> 50	low power switch/chopper	163
2N4392			> 25		
2N4393			> 5		
2N4856	TO-18	40	> 50	low power switch/chopper	167
2N4857		40	> 20		
2N4858		40	> 8		
2N4859		30	> 50		
2N4860		30	> 20		
2N4861		30	> 8		

PRO ELECTRON TYPE DESIGNATION CODE FOR SEMICONDUCTOR DEVICES

This type designation code applies to discrete semiconductor devices – as opposed to integrated circuits –, multiples of such devices and semiconductor chips.

"Although not all type numbers accord with the Pro Electron system, the following explanation is given for the ones that do."

A basic type number consists of:

TWO LETTERS FOLLOWED BY A SERIAL NUMBER

FIRST LETTER

The first letter gives information about the material used for the active part of the devices.

A. GERMANIUM or other material with band gap of 0,6 to 1,0 eV.
B. SILICON or other material with band gap of 1,0 to 1,3 eV.
C. GALLIUM-ARSENIDE or other material with band gap of 1,3 eV or more.
R. COMPOUND MATERIALS (e.g. Cadmium-Sulphide).

SECOND LETTER

The second letter indicates the function for which the device is primarily designed.

A. DIODE; signal, low power
B. DIODE; variable capacitance
C. TRANSISTOR; low power, audio frequency ($R_{th\ j\text{-}mb} > 15\ ^{o}C/W$)
D. TRANSISTOR; power, audio frequency ($R_{th\ j\text{-}mb} \leqslant 15\ ^{o}C/W$)
E. DIODE; tunnel
F. TRANSISTOR; low power, high frequency ($R_{th\ j\text{-}mb} > 15\ ^{o}C/W$)
G. MULTIPLE OF DISSIMILAR DEVICES – MISCELLANEOUS; e.g. oscillator
H. DIODE; magnetic sensitive
L. TRANSISTOR; power, high frequency ($R_{th\ j\text{-}mb} \leqslant 15\ ^{o}C/W$)
N. PHOTO-COUPLER
P. RADIATION DETECTOR; e.g. high sensitivity phototransistor
Q. RADIATION GENERATOR; e.g. light-emitting diode (LED)
R. CONTROL AND SWITCHING DEVICE; e.g. thyristor, low power ($R_{th\ j\text{-}mb} > 15\ ^{o}C/W$)
S. TRANSISTOR; low power, switching ($R_{th\ j\text{-}mb} > 15\ ^{o}C/W$)
T. CONTROL AND SWITCHING DEVICE; e.g. thyristor, power ($R_{th\ j\text{-}mb} \leqslant 15\ ^{o}C/W$)
U. TRANSISTOR; power, switching ($R_{th\ j\text{-}mb} \leqslant 15\ ^{o}C/W$)
X. DIODE: multiplier, e.g. varactor, step recovery
Y. DIODE; rectifying, booster
Z. DIODE; voltage reference or regulator (transient suppressor diode, with third letter W)

SERIAL NUMBER

Three figures, running from 100 to 999, for devices primarily intended for consumer equipment.*
One letter (Z, Y, X, etc.) and two figures, running from 10 to 99, for devices primarily intended for industrial/professional equipment.*
This letter has no fixed meaning except W, which is used for transient suppressor diodes.

VERSION LETTER

It indicates a minor variant of the basic type either electrically or mechanically. The letter never has a fixed meaning, except letter R, indicating reverse voltage, e.g. collector to case or anode to stud.

SUFFIX

Sub-classification can be used for devices supplied in a wide range of variants called associated types. Following sub-coding suffixes are in use:

1. VOLTAGE REFERENCE and VOLTAGE REGULATOR DIODES: *ONE LETTER and ONE NUMBER*
   The LETTER indicates the nominal tolerance of the Zener (regulation, working or reference) voltage
   A. 1% (according to IEC 63: series E96)
   B. 2% (according to IEC 63: series E48)
   C. 5% (according to IEC 63: series E24)
   D. 10% (according to IEC 63: series E12)
   E. 20% (according to IEC 63: series E6)
   The number denotes the typical operating (Zener) voltage related to the nominal current.rating for the whole range.
   The letter 'V' is used instead of the decimal point.

2. TRANSIENT SUPPRESSOR DIODES: *ONE NUMBER*
   The NUMBER indicates the maximum recommended continuous reversed (stand-off) voltage V_R. The letter 'V' is used as above.

3. CONVENTIONAL and CONTROLLED AVALANCHE RECTIFIER DIODES and THYRISTORS: *ONE NUMBER*
   The NUMBER indicates the rated maximum repetitive peak reverse voltage (V_{RRM}) or the rated repetitive peak off-state voltage (V_{DRM}), whichever is the lower. Reversed polarity is indicated by letter R, immediately after the number.

4. RADIATION DETECTORS: *ONE NUMBER,* preceded by a hyphen (–)
   The NUMBER indicates the depletion layer in µm. The resolution is indicated by a version LETTER.

5. ARRAY OF RADIATION DETECTORS and GENERATORS: *ONE NUMBER,* preceded by a stroke (/).
   The NUMBER indicates how many basic devices are assembled into the array.

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* When these serial numbers are exhausted the serial number for consumer types may be extended to four figures, and that for industrial types to three figures.

RATING SYSTEMS

The rating systems described are those recommended by the International Electrotechnical Commission (IEC) in its Publication 134.

DEFINITIONS OF TERMS USED

Electronic device. An electronic tube or valve, transistor or other semiconductor device.

Note
This definition excludes inductors, capacitors, resistors and similar components.

Characteristic. A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

Bogey electronic device. An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

Rating. A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

Note
Limiting conditions may be either maxima or minima.

Rating system. The set of principles upon which ratings are established and which determine their interpretation.

Note
The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

DESIGN CENTRE RATING SYSTEM

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

LETTER SYMBOLS FOR TRANSISTORS AND SIGNAL DIODES

based on IEC Publication 148

LETTER SYMBOLS FOR CURRENTS, VOLTAGES AND POWERS

Basic letters

The basic letters to be used are:

I, i = current
V, v = voltage
P, p = power.

Lower-case basic letters shall be used for the representation of instantaneous values which vary with time.
In all other instances upper-case basic letters shall be used.

Subscripts

A, a	Anode terminal
(AV), (av)	Average value
B, b	Base terminal, for MOS devices: Substrate
(BR)	Breakdown
C, c	Collector terminal
D, d	Drain terminal
E, e	Emitter terminal
F, f	Forward
G, g	Gate terminal
K, k	Cathode terminal
M, m	Peak value
O, o	As third subscript: The terminal not mentioned is open circuited
R, r	As first subscript: Reverse. As second subscript: Repetitive. As third subscript: With a specified resistance between the terminal not mentioned and the reference terminal.
(RMS), (rms)	R.M.S. value
S, s	As first or second subscript: Source terminal (for FETS only) As second subscript: Non-repetitive (not for FETS) As third subscript: Short circuit between the terminal not mentioned and the reference terminal
X, x	Specified circuit
Z, z	Replaces R to indicate the actual working voltage, current or power of voltage reference and voltage regulator diodes.

Note: No additional subscript is used for d.c. values.

Upper-case subscripts shall be used for the indication of:

a) continuous (d.c.) values (without signal)
Example I_B

b) instantaneous total values
Example i_B

c) average total values
Example $I_{B(AV)}$

d) peak total values
Example I_{BM}

e) root-mean-square total values
Example $I_{B(RMS)}$

Lower-case subscripts shall be used for the indication of values applying to the varying component alone:

a) instantaneous values
Example i_b

b) root-mean-square values
Example $I_{b(rms)}$

c) peak values
Example I_{bm}

d) average values
Example $I_{b(av)}$

Note: If more than one subscript is used, subscript for which both styles exist shall either be all upper-case or all lower-case.

Additional rules for subscripts

Subscripts for currents

Transistors: If it is necessary to indicate the terminal carrying the current, this should be done by the first subscript (conventional current flow from the external circuit into the terminal is positive).

Examples: I_B, i_B, i_b, I_{bm}

Diodes: To indicate a forward current (conventional current flow into the anode terminal) the subscript F or f should be used; for a reverse current (conventional current flow out of the anode terminal) the subscript R or r should be used.

Examples: I_F, I_R, i_F, $I_{f(rms)}$

Subscripts for voltages

Transistors: If it is necessary to indicate the points between which a voltage is measured, this should be done by the first two subscripts. The first subscript indicates the terminal at which the voltage is measured and the second the reference terminal or the circuit node. Where there is no possibility of confusion, the second subscript may be omitted.

Examples: V_{BE}, v_{BE}, v_{be}, V_{bem}

Diodes: To indicate a forward voltage (anode positive with respect to cathode), the subscript F or f should be used; for a reverse voltage (anode negative with respect to cathode) the subscript R or r should be used.

Examples: V_F, V_R, v_F, V_{rm}

Subscripts for supply voltages or supply currents

Supply voltages or supply currents shall be indicated by repeating the appropriate terminal subscript.

Examples: V_{CC}, I_{EE}

Note: If it is necessary to indicate a reference terminal, this should be done by a third subscript

Example : V_{CCE}

Subscripts for devices having more than one terminal of the same kind

If a device has more than one terminal of the same kind, the subscript is formed by the appropriate letter for the terminal followed by a number; in the case of multiple subscripts, hyphens may be necessary to avoid misunderstanding.

Examples: I_{B2} = continuous (d.c.) current flowing into the second base terminal

V_{B2-E} = continuous (d.c.) voltage between the terminals of second base and emitter

Subscripts for multiple devices

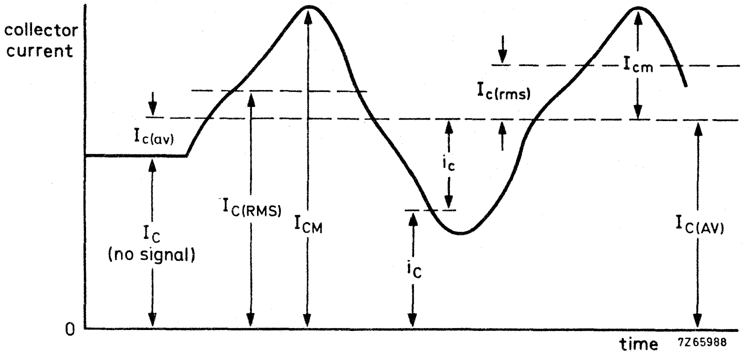
For multiple unit devices, the subscripts are modified by a number preceding the letter subscript; in the case of multiple subscripts, hyphens may be necessary to avoid misunderstanding.

Examples: I_{2C} = continuous (d.c.) current flowing into the collector terminal of the second unit

V_{1C-2C} = continuous (d.c.) voltage between the collector terminals of the first and the second unit.

Application of the rules

The figure below represents a transistor collector current as a function of time. It consists of a continuous (d.c.) current and a varying component.



LETTER SYMBOLS FOR ELECTRICAL PARAMETERS

Definition

For the purpose of this Publication, the term "electrical parameter" applies to four-pole matrix parameters, elements of electrical equivalent circuits, electrical impedances and admittances, inductances and capacitances.

Basic letters

The following is a list of the most important basic letters used for electrical parameters of semiconductor devices.

B, b = susceptance; imaginary part of an admittance
C = capacitance
G, g = conductance; real part of an admittance
H, h = hybrid parameter
L = inductance
R, r = resistance; real part of an impedance
X, x = reactance; imaginary part of an impedance
Y, y = admittance;
Z, z = impedance;

Upper-case letters shall be used for the representation of:

a) electrical parameters of external circuits and of circuits in which the device forms only a part;

b) all inductances and capacitances.

Lower-case letters shall be used for the representation of electrical parameters inherent in the device (with the exception of inductances and capacitances).

Subscripts

General subscripts

The following is a list of the most important general subscripts used for electrical parameters of semiconductor devices:

F, f = forward; forward transfer
I, i (or 1) = input
L, l = load
O, o (or 2) = output
R, r = reverse; reverse transfer
S, s = source

Examples: Z_S, h_f, h_F

The upper-case variant of a subscript shall be used for the designation of static (d.c.) values.

Examples : h_{FE} = static value of forward current transfer ratio in common-emitter configuration (d.c. current gain)
R_E = d.c. value of the external emitter resistance.

Note: The static value is the slope of the line from the origin to the operating point on the appropriate characteristic curve, i.e. the quotient of the appropriate electrical quantities at the operating point.

The lower-case variant of a subscript shall be used for the designation of small-signal values.

Examples: h_{fe} = small-signal value of the short-circuit forward current transfer ratio in common-emitter configuration
$Z_e = R_e + jX_e$ = small-signal value of the external impedance

Note: If more than one subscript is used, subscripts for which both styles exist shall either be all upper-case or all lower-case

Examples: h_{FE}, y_{RE}, h_{fe}

Subscripts for four-pole matrix parameters

The first letter subscript (or double numeric subscript) indicates input, output, forward transfer or reverse transfer

Examples: h_i (or h_{11})
h_o (or h_{22})
h_f (or h_{21})
h_r (or h_{12})

A further subscript is used for the identification of the circuit configuration. When no confusion is possible, this further subscript may be omitted.

Examples: h_{fe} (or h_{21e}), h_{FE} (or h_{21E})

Distinction between real and imaginary parts

If it is necessary to distinguish between real and imaginary parts of electrical parameters, no additional subscripts should be used. If basic symbols for the real and imaginary parts exist, these may be used.

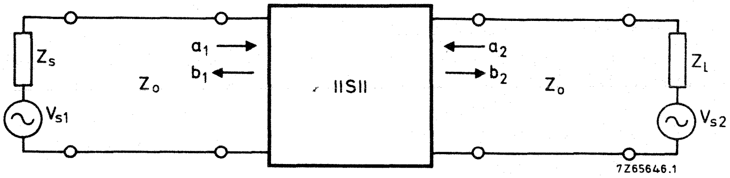
Examples: $Z_i = R_i + jX_i$
$y_{fe} = g_{fe} + jb_{fe}$

If such symbols do not exist or if they are not suitable, the following notation shall be used:

Examples: Re (h_{ib}) etc. for the real part of h_{ib}
Im (h_{ib}) etc. for the imaginary part of h_{ib}

SCATTERING PARAMETERS

In distinction to the conventional h, y and z-parameters, s-parameters relate to travelling wave conditions. The figure below shows a two-port network with the incident and reflected waves a_1, b_1, a_2 and b_2.



$$a_1 = \frac{V_{i1}}{\sqrt{Z_o}} \qquad a_2 = \frac{V_{i2}}{\sqrt{Z_o}}$$

$$b_1 = \frac{V_{r1}}{\sqrt{Z_o}} \qquad b_2 = \frac{V_{r2}}{\sqrt{Z_o}} \qquad ^{1)}$$

Z_o = characteristic impedance of the transmission line in which the two-port is connected.

V_i = incident voltage

V_r = reflected (generated) voltage

The four-pole equations for s-parameters are:

$$b_1 = s_{11}a_1 + s_{12}a_2$$
$$b_2 = s_{21}a_1 + s_{22}a_2$$

Using the subscripts i for 11, r for 12, f for 21 and o for 22, it follows that:

$$s_i = s_{11} = \left.\frac{b_1}{a_1}\right| a_2 = 0$$
$$s_r = s_{12} = \left.\frac{b_1}{a_2}\right| a_1 = 0$$
$$s_f = s_{21} = \left.\frac{b_2}{a_1}\right| a_2 = 0$$
$$s_o = s_{22} = \left.\frac{b_2}{a_2}\right| a_1 = 0$$

---

1) The squares of these quantities have the dimension of power.

The s-parameters can be named and expressed as follows:

$s_i = s_{11}$ = Input reflection coefficient.
The complex ratio of the reflected wave and the incident wave at the input, under the conditions $Z_l = Z_o$ and $V_{s2} = 0$.

$s_r = s_{12}$ = Reverse transmission coefficient.
The complex ratio of the generated wave at the input and the incident wave at the output, under the conditions $Z_s = Z_o$ and $V_{s1} = 0$.

$s_f = s_{21}$ = Forward transmission coefficient.
The complex ratio of the generated wave at the output and the incident wave at the input, under the conditions $Z_l = Z_o$ and $V_{s2} = 0$

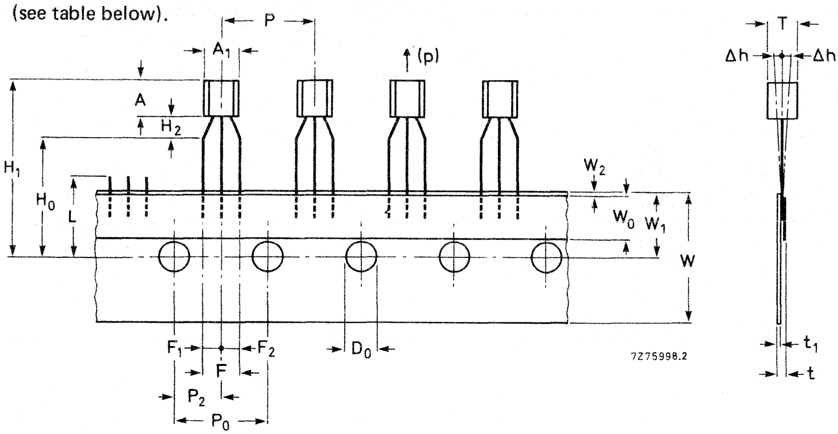
$s_o = s_{22}$ = Output reflection coefficient.
The complex ratio of the reflected wave and the incident wave at the output, under the conditions $Z_s = Z_o$ and $V_{s1} = 0$.

TO-92 VARIANT TRANSISTORS ON TAPE

MECHANICAL DATA

Dimensions in mm

Fig. 1 (see table below).



Item	Symbol	Specifications				Remarks
		min.	nom.	max.	tol.	
Body width	A_1	4,0		4,8		
Body height	A	4,8		5,2		
Body thickness	T	3,9		4,2		
Pitch of component	P		12,7		± 1	
Feed hole pitch	P_o		12,7		± 0,3	Cumulative pitch error 1,0 mm/20 pitch
Feed hole centre to component centre	P_2		6,35		± 0,4	To be measured at bottom of clinch
Distance between outer leads	F		5,08		$+0,6$ $-0,2$	
Component alignment	Δh		0	1		At top of body
Tape width	W		18		± 0,5	
Hold-down tape width	W_o		6		± 0,2	
Hole position	W_1		9		$+0,7$ $-0,5$	
Hold-down tape position	W_2		0,5		± 0,2	
Lead wire clinch height	H_o		16		± 0,5	
Component height	H_1			32,25		
Length of snipped leads	L			11,0		
Feed hole diameter	D_o		4		± 0,2	
Total tape thickness	t			1,2		t_1 0,3-0,6
Lead-to-lead distance	F_1, F_2		2,54		$+0,4$ $-0,1$	
Clinch height	H_2			3		
Pull-out force	(p)	6N				

PACKING

The transistors are supplied on tape in boxes (ammopack) or on reels. The number per reel is 1600 and per ammobox 2000*.

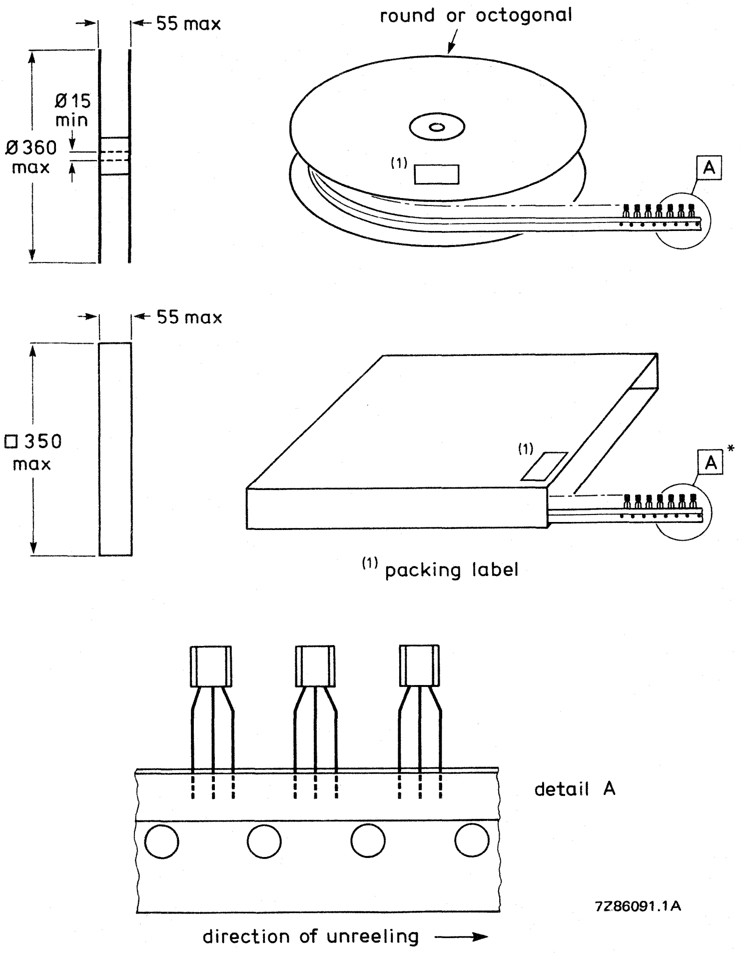


Fig. 2 Dimensions (in mm) of reel and box.

DROPOUTS

A maximum of 0,5% of the specified number of transistors in each packing may be missing. Up to 3 consecutive components may be missing provided the gap is followed by 6 consecutive components.

TAPE SPLICING

Slice the carrier tape on the back and/or front so that the feed hole pitch (P_0) is maintained (see Fig. 3).

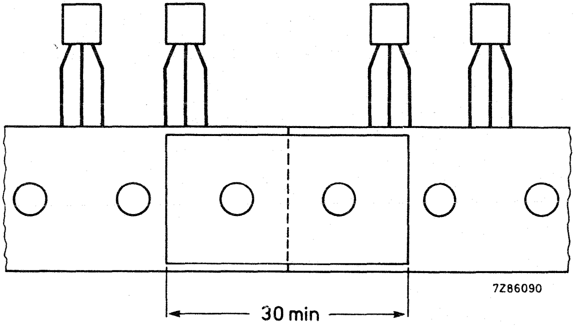


Fig. 3 Jointing tape with splicing patch.

* The ammobox has 80 layers of 25 transistors each.
Each layer contains 25 transistors plus one empty position in order to fold the layer correctly.
The ammobox is accessible from both sides enabling the user to choose between "normal" (see Fig. 2) and "reverse" tape.

SOLDERING RECOMMENDATIONS

SOT-23, SOT-143 AND SOT-89 ENVELOPES

SOT-23, SOT-143 and SOT-89 devices are ideally suited for placement onto thick and thin film substrates and printed circuit boards.

To assure reliable and consistent connections particular attention should be paid to:

1. **Flux**

   A non-active flux is recommended. Where active fluxes are employed, great care in subsequent substrate cleaning must be exercised.

2. **Metal-alloy solder or solder paste**

   Correct choice of solder alloy or solder paste to be employed e.g. 62% Sn, 36% Pb, 2% Ag or 60% Sn/40% Pb. Any paste used should contain at least 85% metal dry weight.

3. **Soldering temperature**

   This will vary according to the actual method employed.

REFLOW SOLDERING

The preferred technique for mounting microminiature components on hybrid thick and thin-film is the method of reflow soldering.

The tags of SOT-23, SOT-143 and SOT-89 envelopes are pre-tinned and the best results are obtained if a similar solder is applied to the corresponding soldering areas on the substrate. This can be done by either dipping the substrate in a solder bath or by screen printing a solder paste.
The maximum temperature of the leads or tab during the soldering cycle should not exceed 285 °C.
The most economic method of soldering is a process in which all different components are soldered simultaneously for example SOT-23, SOT-143 or SOT-89 devices, capacitors and resistors.

Having first been fluxed, all components are positioned on the substrate. The slight adhesive force of the flux is sufficient to keep the components in place. Solder paste contains a flux and has therefore good inherent adhesive properties which eases positioning of the components.

With the components in position the substrate is heated to a point where the solder begins to flow. This can be done on a heating plate or on a conveyor belt running through an infrared tunnel. The maximum allowed temperature of the plastic body of a device must be kept below 280 °C during the soldering cycle. For further temperature behaviour during the soldering process see Figs 2 and 3.

The surface tension of the liquid solder tends to draw the tags of the device towards the centre of the soldering area and has thus a correcting effect on slight mispositionings. However, if the layout leaves something to be desired the same effect can result in undesirable shifts; particularly if the soldering areas on the substrate and the components are not concentrally arranged. This problem can be solved using a standard contact pattern, which leaves sufficient scope for the self-positioning effect (see Figs 4 and 5).

After cooling the connections may be visually inspected and, where necessary, repaired with a light soldering iron. Finally any remaining flux must be removed carefully.

IMMERSION SOLDERING

Where a complete substrate or printed circuit board is immersed in solder:

a. The temperature of the soldering bath should not exceed 280 °C.
b. The duration of the soldering cycle should not exceed 10 seconds.
c. Forced cooling may be applied (see Fig. 1).

HAND SOLDERING

It is possible to solder microminiature devices with a light hand-held soldering iron, but this method has obvious drawbacks and should therefore be restricted to laboratory use and/or incidental repairs on production circuits.

1. It is time-consuming and expensive.
2. The device cannot be positioned accurately and therefore the connecting tags may come into contact with the substrate and damage it.
3. There is a great risk of breaking either substrate or even internal connections inside the encapsulation.
4. The envelope may be damaged by the iron.

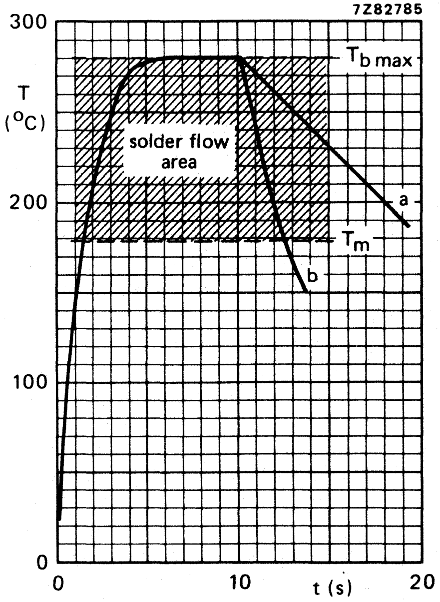
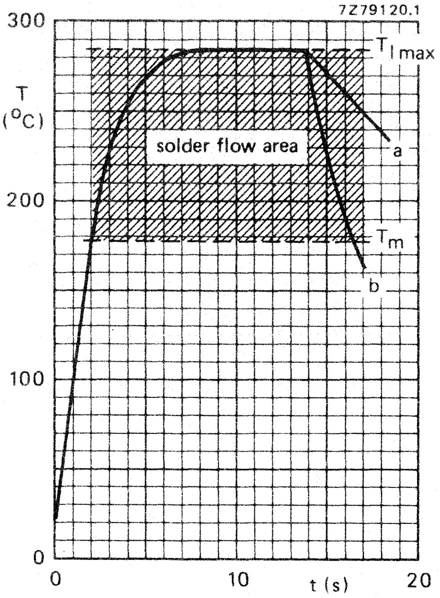


Fig. 1 Device temperature during *immersion* soldering.

Maximum time of immersion in soldering bath is 10 seconds at an ambient temperature of 25 °C.
a = free convection cooling; b = forced cooling.
$T_{b\,max}$ = maximum bath temperature (280 °C).
T_m = melting temperature of solder (179 °C).



a = free convection cooling.

b = permissible forced cooling.

$T_{l\ max}$ = Maximum lead or tab temperature = 285 °C.

T_m = Melting point of the solder is 179 °C.

T_{amb} = 25 °C.

Time of heat supply:
without preheating max. 14 s
with preheating max. 10 s

Maximum time of preheating 45 s

Fig. 2 Reflow soldering without preheating.

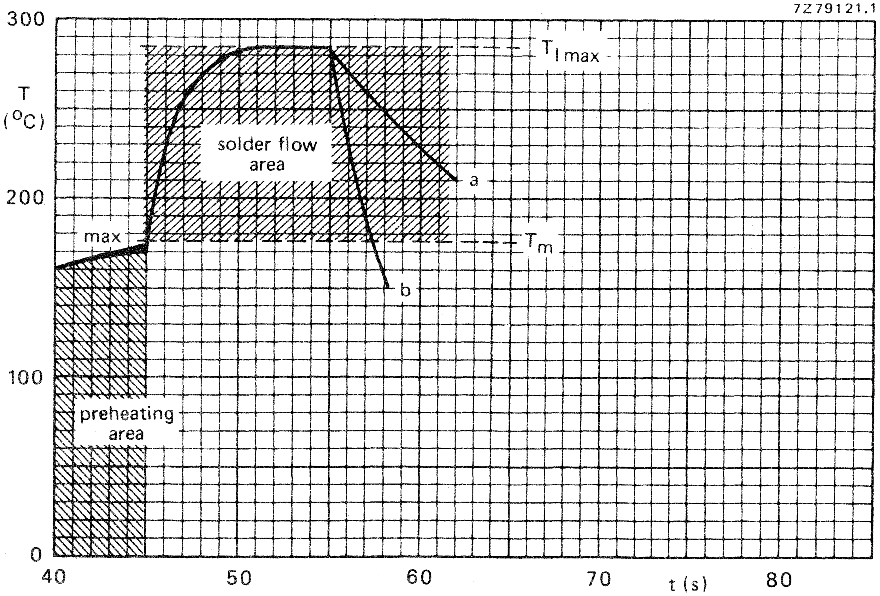


Fig. 3 Reflow soldering with preheating.

Minimum required dimensions of metal connection pads on hybrid thick and thin-film substrates.

Dimensions in mm

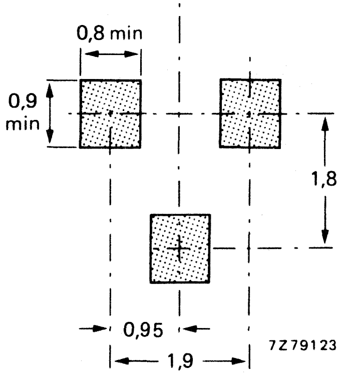


Fig. 4 SOT-23 pattern.

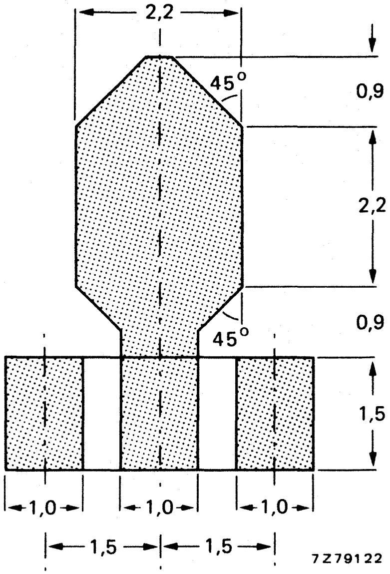


Fig. 5 SOT-89 pattern.

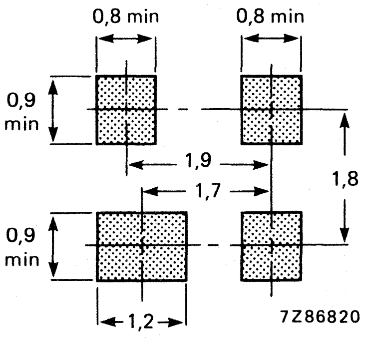


Fig. 6 SOT-143 pattern.

THERMAL CHARACTERISTICS
OF SOT-23 AND SOT-143 ENVELOPES

The heat generated in a semiconductor chip normally flows by various paths to the surroundings (ambient).

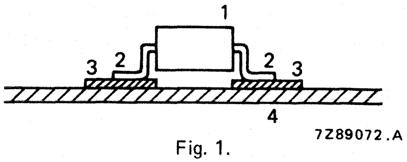


Fig. 1.

1. Heat radiation from the envelope to ambient (1).
   This heat transfer can be neglected when the envelope is mounted on a substrate or printed circuit board.
2. Heat transmission via leads (2) soldering points (3) and substrate (4).

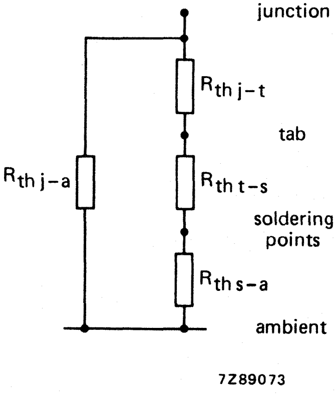


Fig. 2 Thermal behaviour of heat flow when the device is mounted on a substrate or printed circuit board.

$R_{th\,j\text{-}t}$ = Thermal resistance from junction to tab.

$R_{th\,t\text{-}s}$ = Thermal resistance from tab to soldering points.

$R_{th\,s\text{-}a}$ = Thermal resistance from soldering points to ambient.

$R_{th\,j\text{-}a}$ = Thermal resistance from junction to ambient.

The values for the thermal resistance from junction to tab, and tab to soldering points, are mentioned on page 2 and Fig. 5.
The formula for devices in SOT-23 with one crystal can be generalized:

$$T_j = P\,(R_{th\ j\text{-}t} + R_{th\ t\text{-}s} + R_{th\ s\text{-}a}) + T_{amb}$$

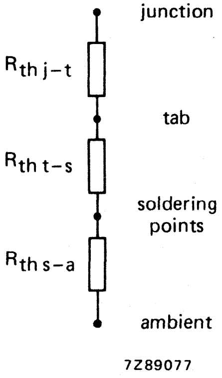


Fig. 6 Thermal model of SOT-23 envelopes with one crystal.

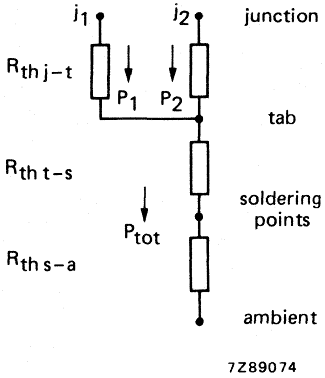


Fig. 7 Thermal model of SOT-23 envelopes with two crystals (double diode).

The formulae for devices with two crystals (double diodes) are:

$$T_{tab} = P_{tot} \cdot (R_{th\ t\text{-}s} + R_{th\ s\text{-}a}) + T_{amb} = P_{tot}\,(280 + 90) + T_{amb}$$

$$T_{j1} = (P_1 \times R_{th\ j\text{-}t}) + T_{tab} = P_1 \cdot 60 + T_{tab}$$

$$T_{j2} = (P_2 \times R_{th\ j\text{-}t}) + T_{tab} = P_2 \cdot 60 + T_{tab}$$

As mentioned on page 2:

$R_{th\ j\text{-}t}$ for diodes is 60 K/W.

$R_{th\ s\text{-}a}$ (area 8 mm x 10 mm x 0,7 mm) = 90 K/W.

$R_{th\ t\text{-}s}$ for all semiconductors in SOT-23 = 280 K/W.

Thus:

$$T_{j1} = 60\,P_1 + 370\,P_{tot} + T_{amb}.$$

$$T_{j2} = 60\,P_2 + 370\,P_{tot} + T_{amb}.$$

Subscripts for voltages

Transistors: If it is necessary to indicate the points between which a voltage is measured, this should be done by the first two subscripts. The first subscript indicates the terminal at which the voltage is measured and the second the reference terminal or the circuit node. Where there is no possibility of confusion, the second subscript may be omitted.

Examples: V_{BE}, v_{BE}, v_{be}, V_{bem}

Diodes: To indicate a forward voltage (anode positive with respect to cathode), the subscript F or f should be used; for a reverse voltage (anode negative with respect to cathode) the subscript R or r should be used.

Examples: V_F, V_R, v_F, V_{rm}

Subscripts for supply voltages or supply currents

Supply voltages or supply currents shall be indicated by repeating the appropriate terminal subscript.

Examples: V_{CC}, I_{EE}

Note: If it is necessary to indicate a reference terminal, this should be done by a third subscript

Example : V_{CCE}

Subscripts for devices having more than one terminal of the same kind

If a device has more than one terminal of the same kind, the subscript is formed by the appropriate letter for the terminal followed by a number; in the case of multiple subscripts, hyphens may be necessary to avoid misunderstanding.

Examples: I_{B2} = continuous (d.c.) current flowing into the second base terminal

V_{B2-E} = continuous (d.c.) voltage between the terminals of second base and emitter

Subscripts for multiple devices

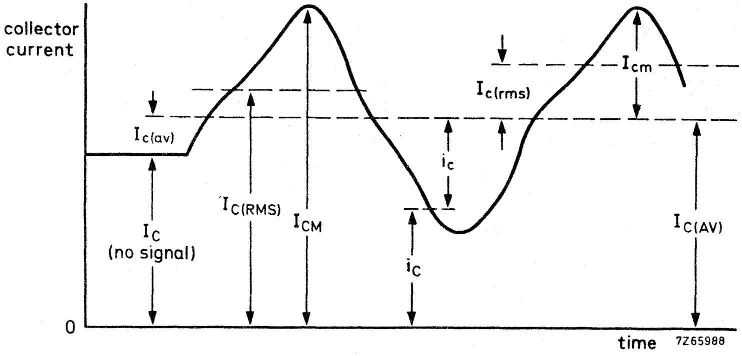
For multiple unit devices, the subscripts are modified by a number preceding the letter subscript; in the case of multiple subscripts, hyphens may be necessary to avoid misunderstanding.

Examples: I_{2C} = continuous (d.c.) current flowing into the collector terminal of the second unit

V_{1C-2C} = continuous (d.c.) voltage between the collector terminals of the first and the second unit.

Application of the rules

The figure below represents a transistor collector current as a function of time. It consists of a continuous (d.c.) current and a varying component.



LETTER SYMBOLS FOR ELECTRICAL PARAMETERS

Definition

For the purpose of this Publication, the term "electrical parameter" applies to four-pole matrix parameters, elements of electrical equivalent circuits, electrical impedances and admittances, inductances and capacitances.

Basic letters

The following is a list of the most important basic letters used for electrical parameters of semiconductor devices.

B, b = susceptance; imaginary part of an admittance

C = capacitance

G, g = conductance; real part of an admittance

H, h = hybrid parameter

L = inductance

R, r = resistance; real part of an impedance

X, x = reactance; imaginary part of an impedance

Y, y = admittance;

Z, z = impedance;

Upper-case letters shall be used for the representation of:

a) electrical parameters of external circuits and of circuits in which the device forms only a part;

b) all inductances and capacitances.

Lower-case letters shall be used for the representation of electrical parameters inherent in the device (with the exception of inductances and capacitances).

Subscripts

General subscripts

The following is a list of the most important general subscripts used for electrical parameters of semiconductor devices:

F, f = forward; forward transfer
I, i (or 1) = input
L, l = load
O, o (or 2) = output
R, r = reverse; reverse transfer
S, s = source

Examples: Z_S, h_f, h_F

The upper-case variant of a subscript shall be used for the designation of static (d.c.) values.

Examples : h_{FE} = static value of forward current transfer ratio in common-emitter configuration (d.c. current gain)
R_E = d.c. value of the external emitter resistance.

Note: The static value is the slope of the line from the origin to the operating point on the appropriate characteristic curve, i.e. the quotient of the appropriate electrical quantities at the operating point.

The lower-case variant of a subscript shall be used for the designation of small-signal values.

Examples: h_{fe} = small-signal value of the short-circuit forward current transfer ratio in common-emitter configuration
$Z_e = R_e + jX_e$ = small-signal value of the external impedance

Note: If more than one subscript is used, subscripts for which both styles exist shall either be all upper-case or all lower-case

Examples: h_{FE}, y_{RE}, h_{fe}

Subscripts for four-pole matrix parameters

The first letter subscript (or double numeric subscript) indicates input, output, forward transfer or reverse transfer

Examples: h_i (or h_{11})
h_o (or h_{22})
h_f (or h_{21})
h_r (or h_{12})

A further subscript is used for the identification of the circuit configuration. When no confusion is possible, this further subscript may be omitted.

Examples: h_{fe} (or h_{21e}), h_{FE} (or h_{21E})

Distinction between real and imaginary parts

If it is necessary to distinguish between real and imaginary parts of electrical parameters, no additional subscripts should be used. If basic symbols for the real and imaginary parts exist, these may be used.

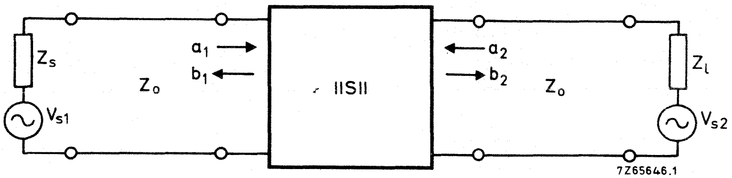
Examples: $Z_i = R_i + jX_i$
$y_{fe} = g_{fe} + jb_{fe}$

If such symbols do not exist or if they are not suitable, the following notation shall be used:

Examples: Re (h_{ib}) etc. for the real part of h_{ib}
Im (h_{ib}) etc. for the imaginary part of h_{ib}

SCATTERING PARAMETERS

In distinction to the conventional h, y and z-parameters, s-parameters relate to travelling wave conditions. The figure below shows a two-port network with the incident and reflected waves a_1, b_1, a_2 and b_2.



$$a_1 = \frac{V_{i1}}{\sqrt{Z_o}} \qquad a_2 = \frac{V_{i2}}{\sqrt{Z_o}}$$

$$b_1 = \frac{V_{r1}}{\sqrt{Z_o}} \qquad b_2 = \frac{V_{r2}}{\sqrt{Z_o}} \qquad {}^{1)}$$

Z_o = characteristic impedance of the transmission line in which the two-port is connected.

V_i = incident voltage

V_r = reflected (generated) voltage

The four-pole equations for s-parameters are:

$$b_1 = s_{11}a_1 + s_{12}a_2$$
$$b_2 = s_{21}a_1 + s_{22}a_2$$

Using the subscripts i for 11, r for 12, f for 21 and o for 22, it follows that:

$$s_i = s_{11} = \left.\frac{b_1}{a_1}\right| a_2 = 0$$
$$s_r = s_{12} = \left.\frac{b_1}{a_2}\right| a_1 = 0$$
$$s_f = s_{21} = \left.\frac{b_2}{a_1}\right| a_2 = 0$$
$$s_o = s_{22} = \left.\frac{b_2}{a_2}\right| a_1 = 0$$

---

1) The squares of these quantities have the dimension of power.

The s-parameters can be named and expressed as follows:

$s_i = s_{11}$ = Input reflection coefficient.
The complex ratio of the reflected wave and the incident wave at the input, under the conditions $Z_l = Z_o$ and $V_{s2} = 0$.

$s_r = s_{12}$ = Reverse transmission coefficient.
The complex ratio of the generated wave at the input and the incident wave at the output, under the conditions $Z_s = Z_o$ and $V_{s1} = 0$.

$s_f = s_{21}$ = Forward transmission coefficient.
The complex ratio of the generated wave at the output and the incident wave at the input, under the conditions $Z_l = Z_o$ and $V_{s2} = 0$

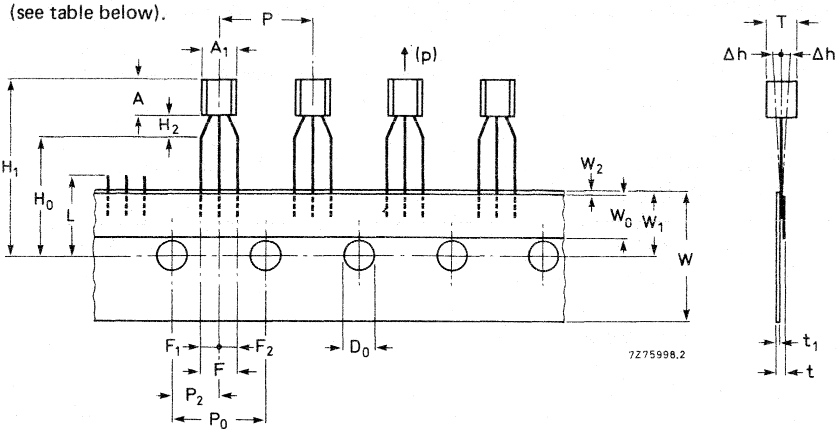
$s_o = s_{22}$ = Output reflection coefficient.
The complex ratio of the reflected wave and the incident wave at the output, under the conditions $Z_s = Z_o$ and $V_{s1} = 0$.

TO-92 VARIANT TRANSISTORS ON TAPE

MECHANICAL DATA

Dimensions in mm

Fig. 1 (see table below).



Item	Symbol	Specifications				Remarks
		min.	nom.	max.	tol.	
Body width	A_1	4,0		4,8		
Body height	A	4,8		5,2		
Body thickness	T	3,9		4,2		
Pitch of component	P		12,7		± 1	
Feed hole pitch	P_o		12,7		± 0,3	Cumulative pitch error 1,0 mm/20 pitch
Feed hole centre to component centre	P_2		6,35		± 0,4	To be measured at bottom of clinch
Distance between outer leads	F		5,08		+ 0,6 −0,2	
Component alignment	Δh		0	1		At top of body
Tape width	W		18		± 0,5	
Hold-down tape width	W_o		6		± 0,2	
Hole position	W_1		9		+ 0,7 −0,5	
Hold-down tape position	W_2		0,5		± 0,2	
Lead wire clinch height	H_o		16		± 0,5	
Component height	H_1			32,25		
Length of snipped leads	L			11,0		
Feed hole diameter	D_o		4		± 0,2	
Total tape thickness	t			1,2		t_1 0,3-0,6
Lead-to-lead distance	F_1, F_2		2,54		+ 0,4 −0,1	
Clinch height	H_2			3		
Pull-out force	(p)	6N				

PACKING

The transistors are supplied on tape in boxes (ammopack) or on reels. The number per reel is 1600 and per ammobox 2000*.

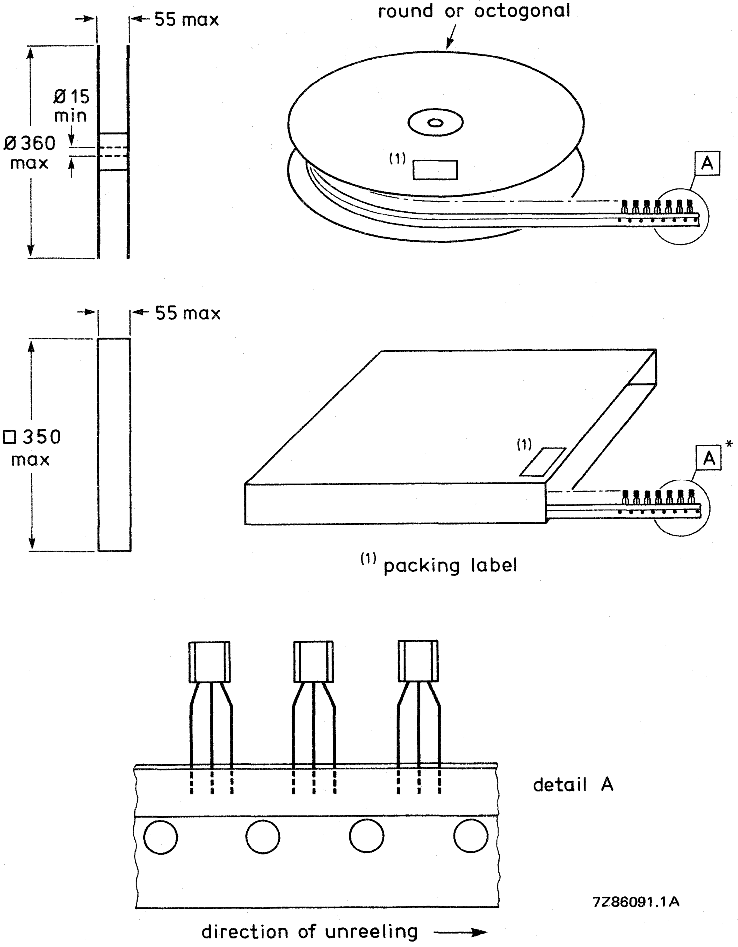


Fig. 2 Dimensions (in mm) of reel and box.

DROPOUTS

A maximum of 0,5% of the specified number of transistors in each packing may be missing. Up to 3 consecutive components may be missing provided the gap is followed by 6 consecutive components.

TAPE SPLICING

Slice the carrier tape on the back and/or front so that the feed hole pitch (P_o) is maintained (see Fig. 3).

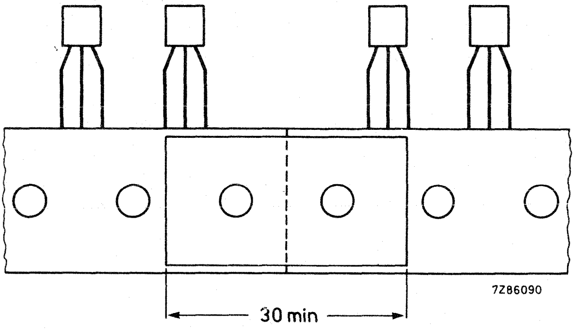


Fig. 3 Jointing tape with splicing patch.

* The ammobox has 80 layers of 25 transistors each.
Each layer contains 25 transistors plus one empty position in order to fold the layer correctly.

The ammobox is accessible from both sides enabling the user to choose between "normal" (see Fig. 2) and "reverse" tape.

SOLDERING RECOMMENDATIONS
SOT-23, SOT-143 AND SOT-89 ENVELOPES

SOT-23, SOT-143 and SOT-89 devices are ideally suited for placement onto thick and thin film substrates and printed circuit boards.

To assure reliable and consistent connections particular attention should be paid to:

1. **Flux**

   A non-active flux is recommended. Where active fluxes are employed, great care in subsequent substrate cleaning must be exercised.

2. **Metal-alloy solder or solder paste**

   Correct choice of solder alloy or solder paste to be employed e.g. 62% Sn, 36% Pb, 2% Ag or 60% Sn/40% Pb. Any paste used should contain at least 85% metal dry weight.

3. **Soldering temperature**

   This will vary according to the actual method employed.

REFLOW SOLDERING

The preferred technique for mounting microminiature components on hybrid thick and thin-film is the method of reflow soldering.

The tags of SOT-23, SOT-143 and SOT-89 envelopes are pre-tinned and the best results are obtained if a similar solder is applied to the corresponding soldering areas on the substrate. This can be done by either dipping the substrate in a solder bath or by screen printing a solder paste.
The maximum temperature of the leads or tab during the soldering cycle should not exceed 285 °C.
The most economic method of soldering is a process in which all different components are soldered simultaneously for example SOT-23, SOT-143 or SOT-89 devices, capacitors and resistors.

Having first been fluxed, all components are positioned on the substrate. The slight adhesive force of the flux is sufficient to keep the components in place. Solder paste contains a flux and has therefore good inherent adhesive properties which eases positioning of the components.

With the components in position the substrate is heated to a point where the solder begins to flow. This can be done on a heating plate or on a conveyor belt running through an infrared tunnel. The maximum allowed temperature of the plastic body of a device must be kept below 280 °C during the soldering cycle. For further temperature behaviour during the soldering process see Figs 2 and 3.

The surface tension of the liquid solder tends to draw the tags of the device towards the centre of the soldering area and has thus a correcting effect on slight mispositionings. However, if the layout leaves something to be desired the same effect can result in undesirable shifts; particularly if the soldering areas on the substrate and the components are not concentrally arranged. This problem can be solved using a standard contact pattern, which leaves sufficient scope for the self-positioning effect (see Figs 4 and 5).

After cooling the connections may be visually inspected and, where necessary, repaired with a light soldering iron. Finally any remaining flux must be removed carefully.

IMMERSION SOLDERING

Where a complete substrate or printed circuit board is immersed in solder:
a. The temperature of the soldering bath should not exceed 280 °C.
b. The duration of the soldering cycle should not exceed 10 seconds.
c. Forced cooling may be applied (see Fig. 1).

HAND SOLDERING

It is possible to solder microminiature devices with a light hand-held soldering iron, but this method has obvious drawbacks and should therefore be restricted to laboratory use and/or incidental repairs on production circuits.

1. It is time-consuming and expensive.
2. The device cannot be positioned accurately and therefore the connecting tags may come into contact with the substrate and damage it.
3. There is a great risk of breaking either substrate or even internal connections inside the encapsulation.
4. The envelope may be damaged by the iron.

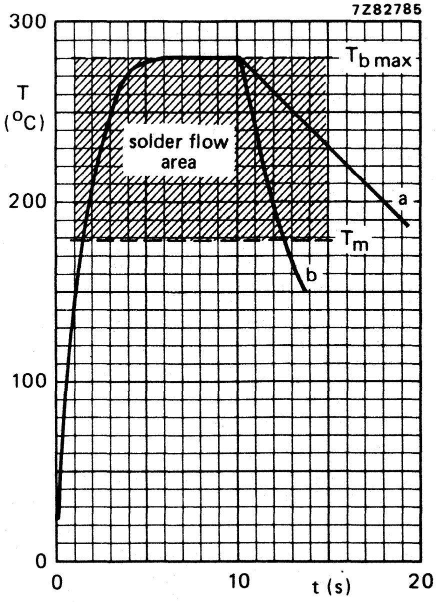
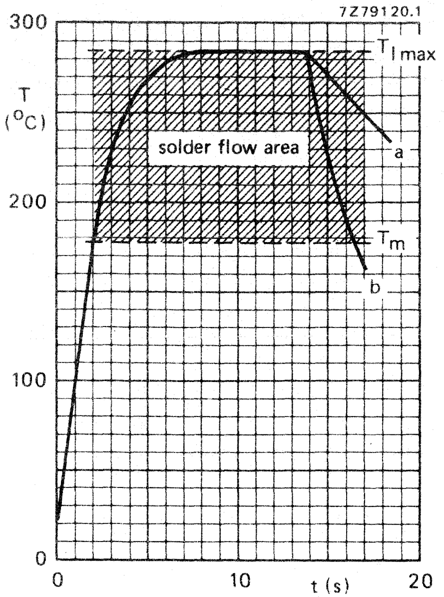


Fig. 1 Device temperature during *immersion* soldering.

Maximum time of immersion in soldering bath is 10 seconds at an ambient temperature of 25 °C.
a = free convection cooling; b = forced cooling.
$T_{b\,max}$ = maximum bath temperature (280 °C).
T_m = melting temperature of solder (179 °C).



a = free convection cooling.

b = permissible forced cooling.

$T_{l\,max}$ = Maximum lead or tab temperature = 285 °C.

T_m = Melting point of the solder is 179 °C.

T_{amb} = 25 °C.

Time of heat supply:
without preheating max. 14 s
with preheating max. 10 s

Maximum time of preheating 45 s

Fig. 2 Reflow soldering without preheating.

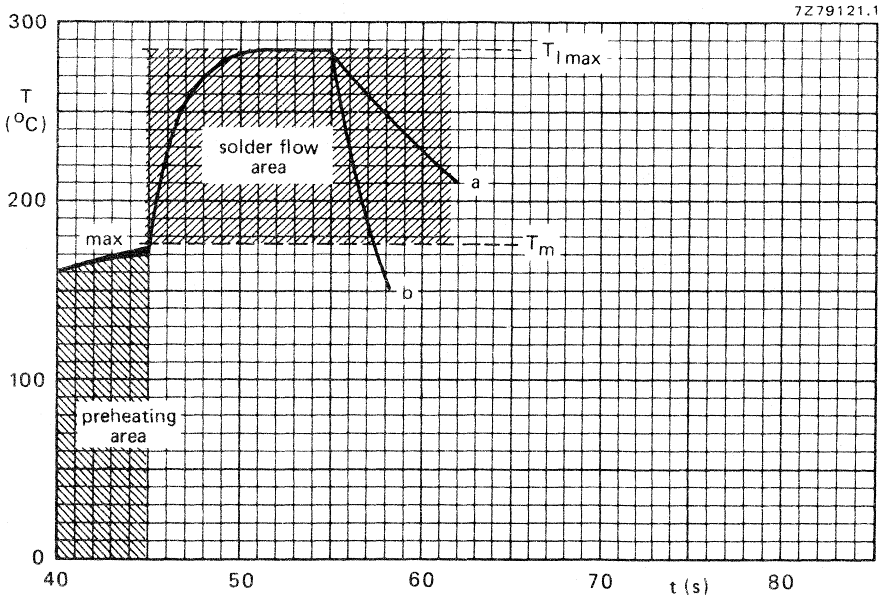


Fig. 3 Reflow soldering with preheating.

Minimum required dimensions of metal connection pads on hybrid thick and thin-film substrates.

Dimensions in mm

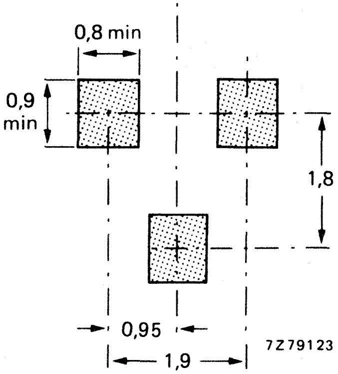


Fig. 4 SOT-23 pattern.

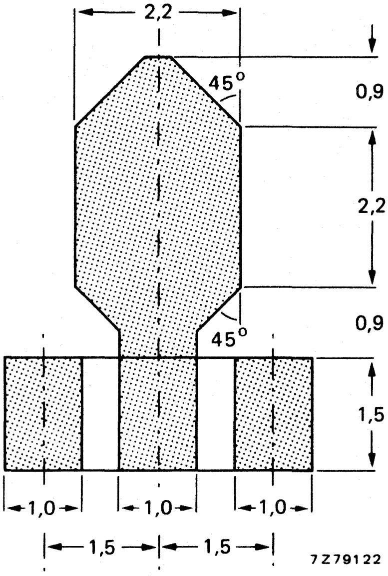


Fig. 5 SOT-89 pattern.

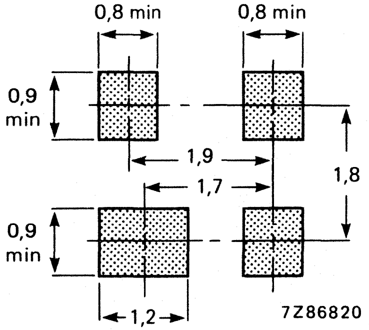


Fig. 6 SOT-143 pattern.

THERMAL CHARACTERISTICS
OF SOT-23 AND SOT-143 ENVELOPES

The heat generated in a semiconductor chip normally flows by various paths to the surroundings (ambient).

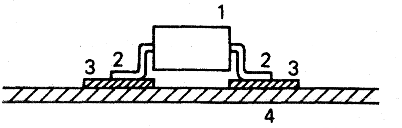


Fig. 1.

1. Heat radiation from the envelope to ambient (1).
   This heat transfer can be neglected when the envelope is mounted on a substrate or printed circuit board.
2. Heat transmission via leads (2) soldering points (3) and substrate (4).

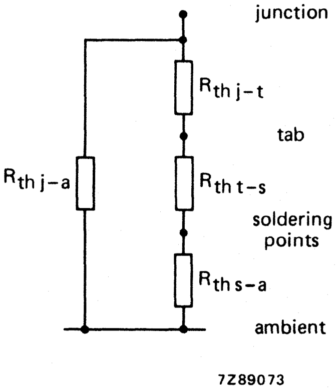


Fig. 2 Thermal behaviour of heat flow when the device is mounted on a substrate or printed circuit board.

$R_{th\,j\text{-}t}$ = Thermal resistance from junction to tab.

$R_{th\,t\text{-}s}$ = Thermal resistance from tab to soldering points.

$R_{th\,s\text{-}a}$ = Thermal resistance from soldering points to ambient.

$R_{th\,j\text{-}a}$ = Thermal resistance from junction to ambient.

The values for the thermal resistance from junction to tab, and tab to soldering points, are mentioned on page 2 and Fig. 5.

The formula for devices in SOT-23 with one crystal can be generalized:

$$T_j = P\,(R_{th\ j\text{-}t} + R_{th\ t\text{-}s} + R_{th\ s\text{-}a}) + T_{amb}$$

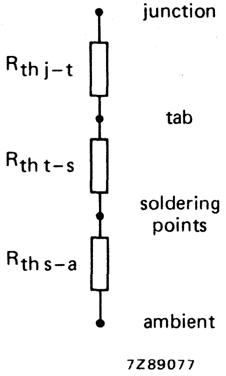


Fig. 6 Thermal model of SOT-23 envelopes with one crystal.

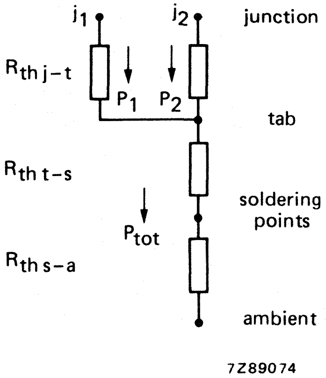


Fig. 7 Thermal model of SOT-23 envelopes with two crystals (double diode).

The formulae for devices with two crystals (double diodes) are:

$$T_{tab} = P_{tot} \cdot (R_{th\ t\text{-}s} + R_{th\ s\text{-}a}) + T_{amb} = P_{tot}\,(280 + 90) + T_{amb}$$

$$T_{j1} = (P_1 \times R_{th\ j\text{-}t}) + T_{tab} = P_1 \cdot 60 + T_{tab}$$

$$T_{j2} = (P_2 \times R_{th\ j\text{-}t}) + T_{tab} = P_2 \cdot 60 + T_{tab}$$

As mentioned on page 2:

$R_{th\ j\text{-}t}$ for diodes is 60 K/W.

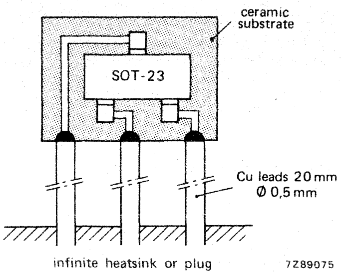
$R_{th\ s\text{-}a}$ (area 8 mm x 10 mm x 0,7 mm) = 90 K/W.

$R_{th\ t\text{-}s}$ for all semiconductors in SOT-23 = 280 K/W.

Thus:

$$T_{j1} = 60\,P_1 + 370\,P_{tot} + T_{amb}.$$

$$T_{j2} = 60\,P_2 + 370\,P_{tot} + T_{amb}.$$



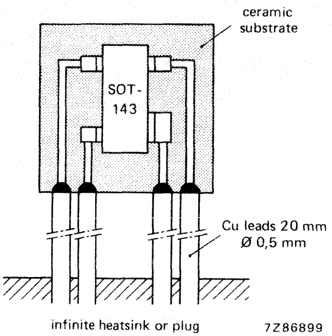


Fig. 4 Test circuits SOT-23 and SOT-143 mounting conditions on a ceramic substrate.

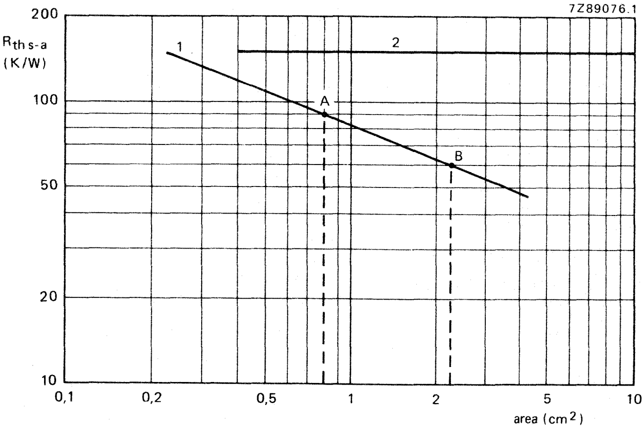


Fig. 5 Heat transfer from soldering points to ambient.

1. Ceramic substrate

Point A on the curve in Fig. 5 is for an area of the ceramic substrate of 8 mm x 10 mm x 0,7 mm for the maximum rating of all high-frequency, low-frequency and switching transistors and also for all diodes.
Point B on the curve in Fig. 5 is for an area of the ceramic substrate of 15 mm x 15 mm x 0,7 mm for the maximum rating of low-frequency medium-power semiconductors.

2. Printed circuit board

$R_{th\ s\text{-}a}$ = 150 K/W for SOT-23 and SOT-143 envelopes mounted on a printed circuit board.

Heat transfer directly from envelope to ambient

This depends on the difference between the temperatures of envelope and the surroundings. When the device is mounted on a substrate or printed circuit board direct heat flow can usually be neglected in relation to the heat flow via leads and substrate.
Thus the thermal model can be as in Fig. 3.

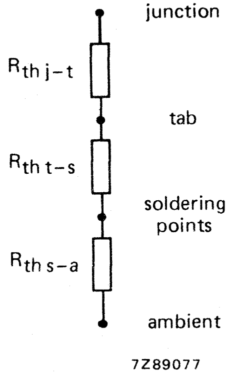


Fig. 3 Basic thermal model.

Heat transfer from junction to tab

This is an internal heat transfer and has been measured. In general it is:

for high-frequency transistors, low-power diodes and (MOS) FETs	60 K/W
for low-frequency and switching transistors	50 K/W
for low-frequency medium-power transistors	30 K/W

Heat transfer from tab to soldering points

This value has also been measured for SOT-23 with $P_{tot} < 350$ mW	280 K/W
for types of semiconductors in this envelope with $P_{tot} < 425$ mW	260 K/W
for types of semiconductors in a SOT-143 envelope this value is	310 K/W

Heat transfer from soldering points to ambient

This depends on the shape and material of tracks and substrate. In figures 4 and 5 standard mounting conditions are given to set up the maximum power ratings for SOT-23 and SOT-143 encapsulations.

SOLDERING RECOMMENDATIONS SOT-37

Transistors in SOT-37 envelopes may be mounted with leads flat (Fig. 1) or bent (Figs 2 and 3). Different soldering procedures apply for the different styles of mounting.

FLAT-LEAD MOUNTING

Soldering by hand

Avoid putting any force on the leads during or just after soldering.

Solder the three leads one at a time, *not* simultaneously.

Proceed from one lead to the adjacent lead, *not* to the opposite one.

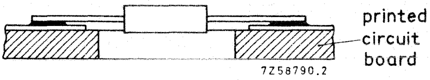


Fig. 1

Solder temperature	max.	300 °C
Soldering time	max.	5 s
Solder-to-case distance	min.	2 mm

BENT-LEAD MOUNTING

If leads are bent, all three may be soldered simultaneously if desired.

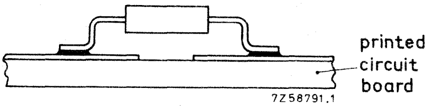


Fig. 2

Solder temperature	max.	300 °C
Soldering time	max.	10 s

DIP OR WAVE SOLDERING

When dip or wave soldering, the maximum allowable temperature of the solder is 260 °C. This temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds. The device may be mounted up to the lead projections, but the temperature of the body must not exceed the specified storage maximum.

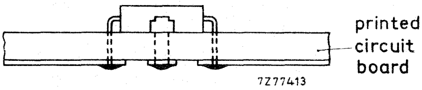


Fig. 3

Solder temperature	max.	260 °C
Soldering time	max.	5 s

SOLDERING RECOMMENDATIONS SOT-103

Transistors in SOT-103 envelopes may be mounted with leads flat (Fig. 1) or bent (Figs 2 and 3). Different soldering procedures apply for the different styles of mounting.

FLAT-LEAD MOUNTING

Soldering by hand

Avoid putting any force on the leads during or just after soldering.

Solder the four leads one at a time, *not* simultaneously.

Proceed from one lead to the adjacent lead, *not* to the opposite one.

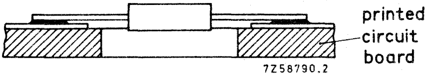


Fig. 1

Solder temperature	max.	300	°C
Soldering time	max.	5	s
Solder-to-case distance	min.	2	mm

BENT-LEAD MOUNTING

If leads are bent, all four may be soldered simultaneously if desired.

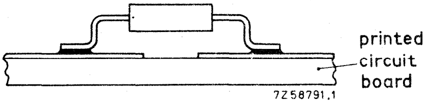


Fig. 2

Solder temperature	max.	300	°C
Soldering time	max.	10	s

DIP OR WAVE SOLDERING

When dip or wave soldering, the maximum allowable temperature of the solder is 260 °C. This temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds. The device may be mounted up to the lead projections, but the temperature of the body must not exceed the specified storage maximum.

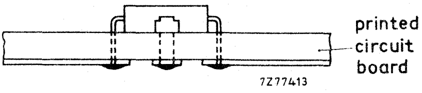


Fig. 3

Solder temperature	max.	260	°C
Soldering time	max.	5	s

DEVICE DATA

J-FETS

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Symmetrical N-channel planar epitaxial junction field-effect transistors in a plastic TO-92 variant; intended for hi-fi amplifiers and other audio-frequency equipment.

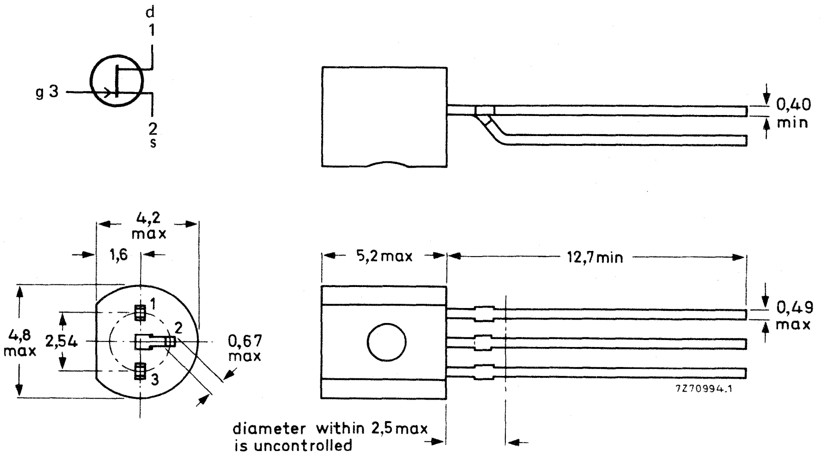
QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Total power dissipation up to $T_{amb} = 25\ ^{o}C$	P_{tot}	max.	300	mW
Junction temperature	T_j	max.	150	^{o}C
Drain current $V_{DS} = 15$ V; $V_{GS} = 0$	I_{DSS}		2 to 12	mA
Transfer admittance (common source) $V_{DS} = 15$ V; $V_{GS} = 0$; f = 1 kHz	$\lvert y_{fs} \rvert$	typ.	3,5	mA/V
Noise figure at $V_{DS} = 15$ V; $V_{GS} = 0$ f = 1 kHz; $R_G = 1\ M\Omega$	F	<	2	dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages				
Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Current				
Gate current	I_G	max.	10	mA
Power dissipation				
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300	mW
Temperatures				
Storage temperature	T_{stg}		−65 to +150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	0, 42	°C/mW

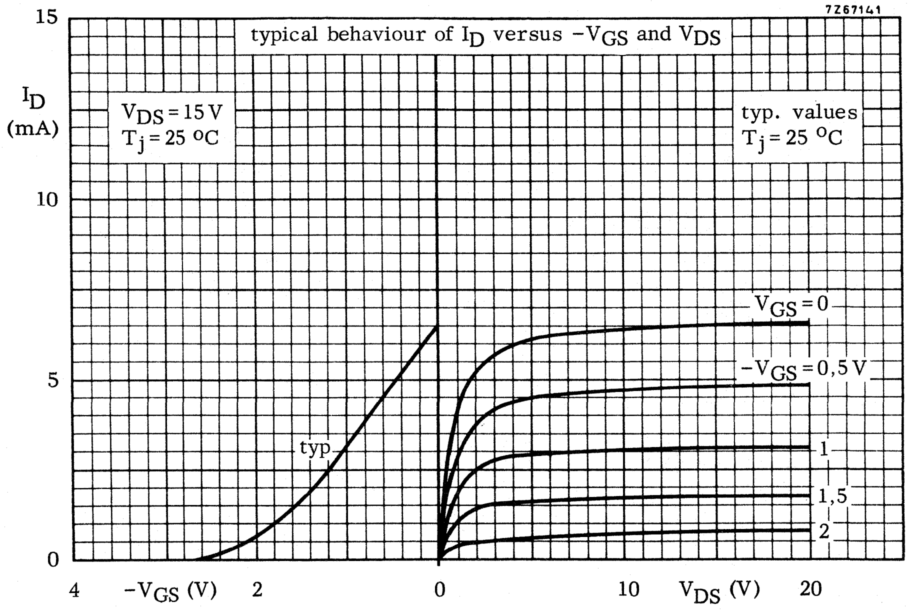
CHARACTERISTICS

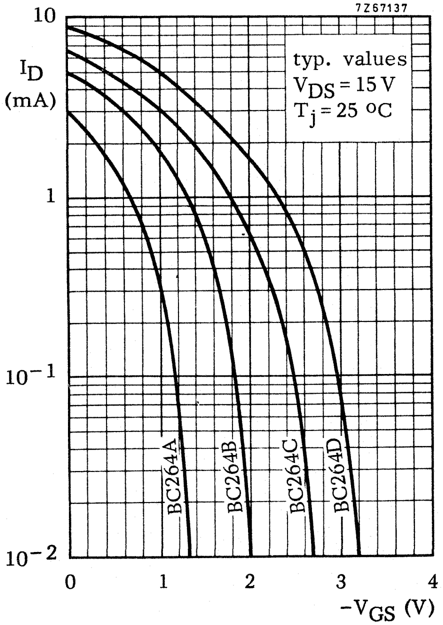
T_j = 25 °C unless otherwise specified

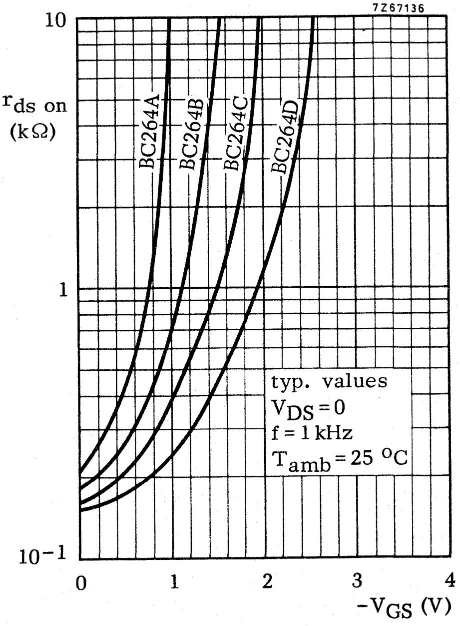
			BC264A	B	C	D	
Gate cut-off current							
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	<	10	10	10	10	nA
Drain current [1]							
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	2,0	3,5	5,0	7,0	mA
		<	4,5	6,5	8,0	12,0	mA
Gate-source breakdown voltage							
$-I_G$ = 1 μA; V_{DS} = 0	$-V_{(BR)GSS}$	>	30	30	30	30	V
Gate-source voltage							
I_D = 200 μA ; V_{DS} = 15 V	$-V_{GS}$	>	0,4	0,4	0,4	0,4	V
I_D = 1,0 mA; V_{DS} = 15 V	$-V_{GS}$	>	0,2	–	–	–	V
		<	1,2	–	–	–	V
I_D = 1,5 mA; V_{DS} = 15 V	$-V_{GS}$	>	–	0,4	–	–	V
		<	–	1,4	–	–	V
I_D = 2,5 mA; V_{DS} = 15 V	$-V_{GS}$	>	–	–	0,5	–	V
		<	–	–	1,5	–	V
I_D = 3,5 mA; V_{DS} = 15 V	$-V_{GS}$	>	–	–	–	0,6	V
		<	–	–	–	1,6	V
Gate-source cut-off voltage							
I_D = 10 nA ; V_{DS} = 15 V	$-V_{(P)GS}$	>	0,5	0,5	0,5	0,5	V
y-parameters at T_{amb} = 25 °C							
V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz							
Transfer admittance	$\|y_{fs}\|$	>	2,5	3,0	3,5	4,0	mA/V
V_{DS} = 15 V; $-V_{GS}$ = 1 V; f = 1 MHz							
Input capacitance	C_{is}	typ.	4,0				pF
Feedback capacitance	C_{rs}	typ.	1,2				pF
Output capacitance	C_{os}	typ.	1,6				pF
Noise figure at f = 1 kHz; R_G = 1 MΩ							
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C	F	typ.	0,5				dB
		<	2				dB
Equivalent noise voltage at T_{amb} = 25 °C							
V_{DS} = 15 V; V_{GS} = 0; f = 10 Hz	$V_n/\sqrt{B}$	typ.	40				nV/$\sqrt{Hz}$

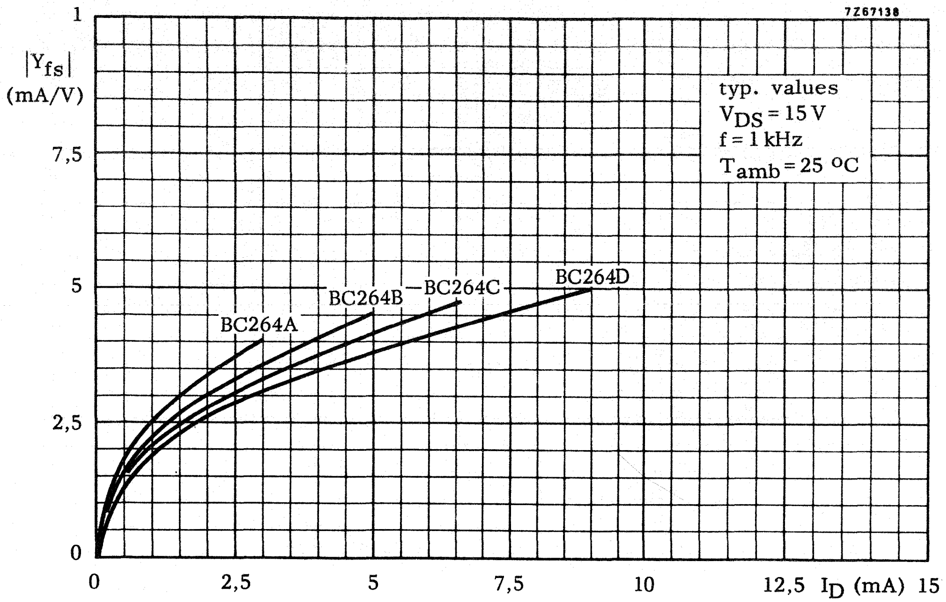
---

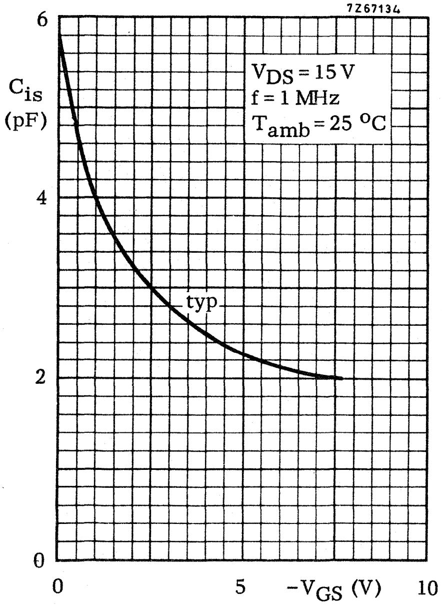
[1] Measured under pulse conditions.

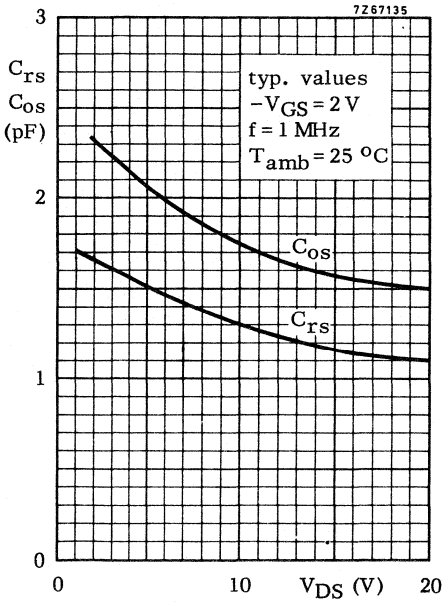

7Z67141
typical behaviour of I_D versus $-V_{GS}$ and V_{DS}
I_D (mA)
15
10
5
0
$V_{DS} = 15$ V
$T_j = 25$ °C
typ. values
$T_j = 25$ °C
typ
$V_{GS} = 0$
$-V_{GS} = 0,5$ V
1
1,5
2
4
$-V_{GS}$ (V)
2
0
10
V_{DS} (V)
20

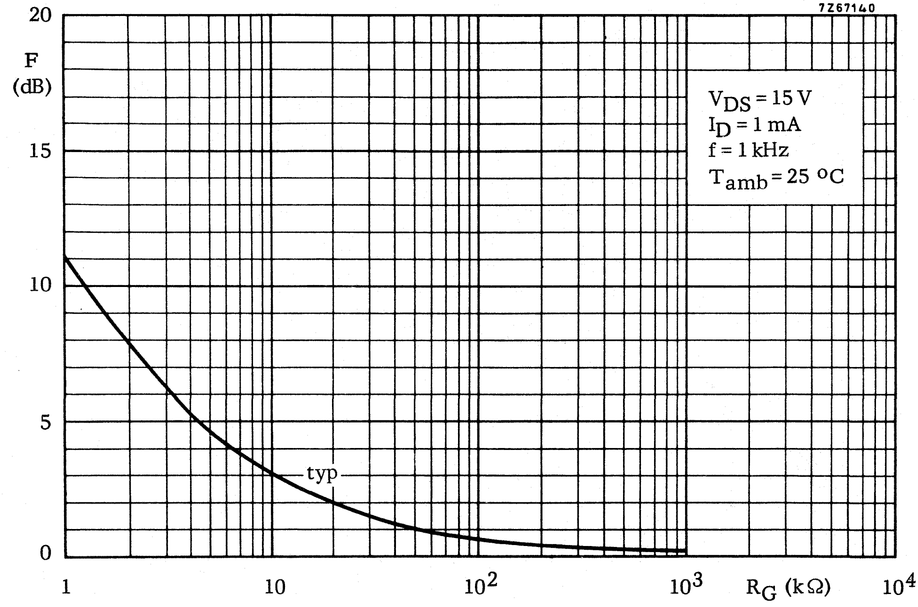

7Z67137
10
I_D (mA)
1
10^{-1}
10^{-2}
typ. values
$V_{DS} = 15$ V
$T_j = 25$ °C
BC264A
BC264B
BC264C
BC264D
0
1
2
3
4
$-V_{GS}$ (V)


7Z67136
10
$r_{ds\ on}$ (kΩ)
1
10^{-1}
BC264A
BC264B
BC264C
BC264D
typ. values
$V_{DS} = 0$
f = 1 kHz
$T_{amb} = 25$ °C
0
1
2
3
4
$-V_{GS}$ (V)


7Z67138
|Y$_{fs}$|
(mA/V)
1
7,5
5
2,5
0
0
2,5
5
7,5
10
12,5
I$_D$ (mA)
15
typ. values
V$_{DS}$ = 15 V
f = 1 kHz
T$_{amb}$ = 25 °C
BC264A
BC264B
BC264C
BC264D


7Z67134
C$_{is}$
(pF)
6
4
2
0
0
5
−V$_{GS}$ (V)
10
V$_{DS}$ = 15 V
f = 1 MHz
T$_{amb}$ = 25 °C
typ


7Z67135
C$_{rs}$
C$_{os}$
(pF)
3
2
1
0
0
10
V$_{DS}$ (V)
20
typ. values
−V$_{GS}$ = 2 V
f = 1 MHz
T$_{amb}$ = 25 °C
C$_{os}$
C$_{rs}$


7Z67140
20
F
(dB)
15
10
5
0
1
10
10^2
10^3
R_G (kΩ)
10^4
V_{DS} = 15 V
I_D = 1 mA
f = 1 kHz
T_{amb} = 25 °C
typ

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

General purpose symmetrical N-channel planar epitaxial junction field-effect transistors in a plastic TO-92 variant; intended for applications in l.f. and d.c. amplifiers, and in h.f. amplifiers.

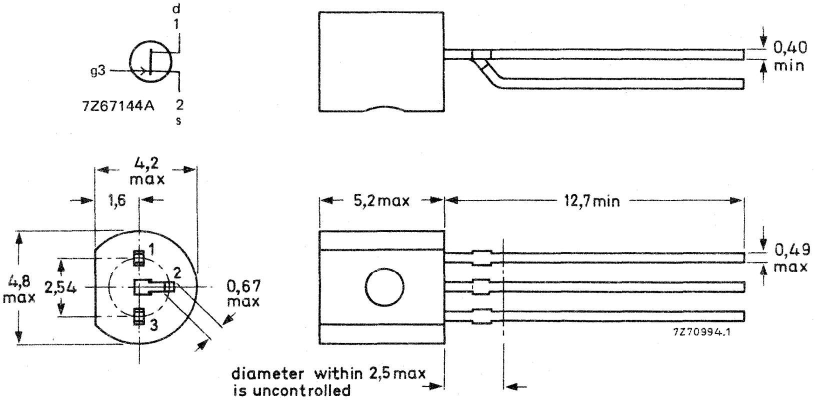
QUICK REFERENCE DATA

			BF245A/0	A	B	C	
Drain-source voltage	$\pm V_{DS}$	max.				30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.				30	V
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.				300	mW
Drain current $V_{DS} = 15$ V; $V_{GS} = 0$	I_{DSS}	>	0,5	2,0	6	12	mA
		<	2,0	6,5	15	25	mA
Gate-source cut-off voltage $I_D = 10$ nA; $V_{DS} = 15$ V	$-V_{(P)GS}$					0,25 to 8,0	V
Feedback capacitance at f = 1 MHz $V_{DS} = 20$ V; $-V_{GS} = 1$ V; $T_{amb} = 25$ °C	C_{rs}	typ.				1,1	pF
Transfer admittance (common source) $V_{DS} = 15$ V; $V_{GS} = 0$; f = 1 kHz; $T_{amb} = 25$ °C	$\lvert y_{fs}\rvert$					3,0 to 6,5	mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30 V
Drain-gate voltage (open source)	V_{DGO}	max.	30 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30 V
Drain current	I_D	max.	25 mA
Gate current	I_G	max.	10 mA
Power dissipation			
up to $T_{amb} = 75\ ^{o}C$	P_{tot}	max.	300 mW
up to $T_{amb} = 90\ ^{o}C$	P_{tot}	max.	300 mW 1)
Storage temperature	T_{stg}	−65 to + 150 °C	
Junction temperature	T_j	max.	150 °C

→ THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\,j\text{-}a}$	=	0,25 K/mW
From junction to ambient	$R_{th\,j\text{-}a}$	=	0,20 K/mW 1)

CHARACTERISTICS

$T_j = 25\ ^{o}C$ unless otherwise specified

			BF245A	B	C	
Gate cut-off current						
$-V_{GS} = 20$ V; $V_{DS} = 0$	$-I_{GSS}$	<	5	5	5	nA
$-V_{GS} = 20$ V; $V_{DS} = 0$; $T_j = 125\ ^{o}C$	$-I_{GSS}$	<	0,5	0,5	0,5	μA
Drain current 2)						
→ $V_{DS} = 15$ V; $V_{GS} = 0$	I_{DSS} 3)	>	2	6,0	12	mA
		<	6,5	15,0	25	mA
Gate-source breakdown voltage						
$-I_G = 1\ \mu$A; $V_{DS} = 0$	$-V_{(BR)GSS}$	>	30	30	30	V
Gate-source voltage						
→ $I_D = 200\ \mu$A; $V_{DS} = 15$ V	$-V_{GS}$ 3)	>	0,4	1,6	3,2	V
		<	2,2	3,8	7,5	V

1) Transistor mounted on printed circuit board, maximum lead length 3 mm, mounting pad for drain lead minimum 10 mm x 10 mm.

2) Measured under pulse conditions: $t_p = 300\ \mu s$; $\delta \leqslant 0{,}02$.

→ 3) BF245A/0: I_{DSS} = 0,5 to 2,0 mA; $-V_{GS}$ = 0,2 to 1,0 V
BF245A/1: I_{DSS} = 2,0 to 3,0 mA; $-V_{GS}$ = 0,4 to 1,0 V
BF245A/2: I_{DSS} = 3,0 to 4,5 mA; $-V_{GS}$ = 0,7 to 1,4 V
BF245A/3: I_{DSS} = 4,5 to 6,5 mA; $-V_{GS}$ = 1,1 to 2,2 V.

Gate-source cut-off voltage			
I_D = 10 nA; V_{DS} = 15 V		$-V_{(P)GS}$	0,25 to 8,0 V ←
y-parameters at T_{amb} = 25 °C (common source)			
V_{DS} = 15 V; V_{GS} = 0			
f = 1 kHz	Transfer admittance	$\lvert y_{fs}\rvert$	3,0 to 6,5 mS
	Output admittance	$\lvert y_{os}\rvert$	typ. 25 µS
f = 200 MHz	Input conductance	g_{is}	typ. 250 µS
	Reverse transfer admittance	$\lvert y_{rs}\rvert$	typ. 1,4 mS
	Transfer admittance	$\lvert y_{fs}\rvert$	typ. 6 mS
	Output conductance	g_{os}	typ. 40 µS
V_{DS} = 20 V; $-V_{GS}$ = 1 V			
f = 1 MHz	Input capacitance	C_{is}	typ. 4,0 pF
	Feedback capacitance	C_{rs}	typ. 1,1 pF
	Output capacitance	C_{os}	typ. 1,6 pF
Cut-off frequency*			
V_{DS} = 15 V; V_{GS} = 0		f_{gfs}	typ. 700 MHz
Noise figure at f = 100 MHz; R_G = 1 kΩ (common source)			
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C input tuned to minimum noise		F	typ. 1,5 dB

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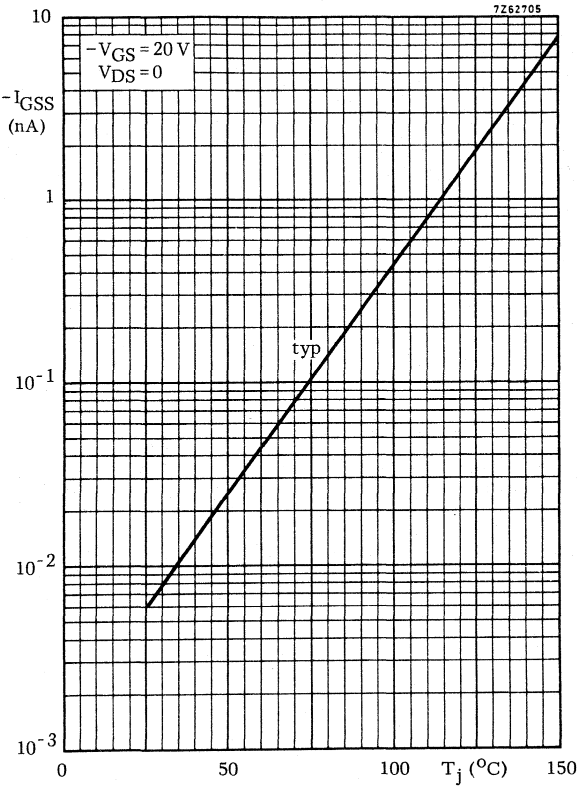
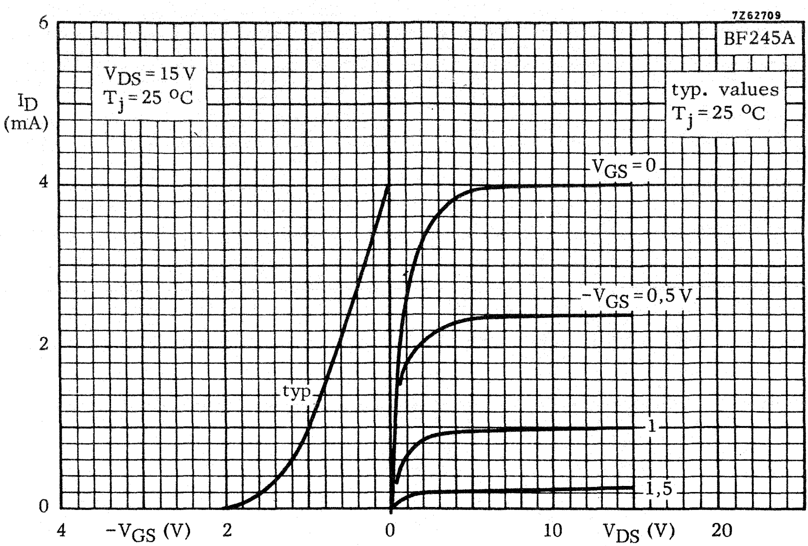
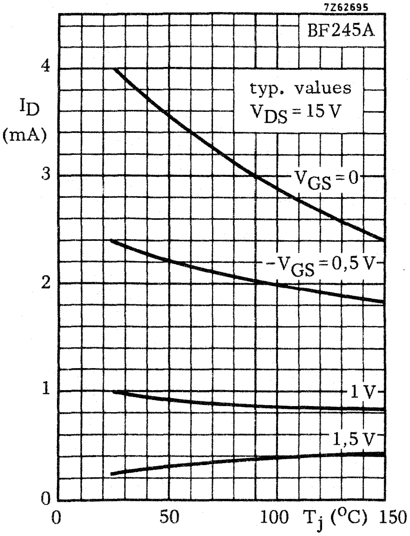
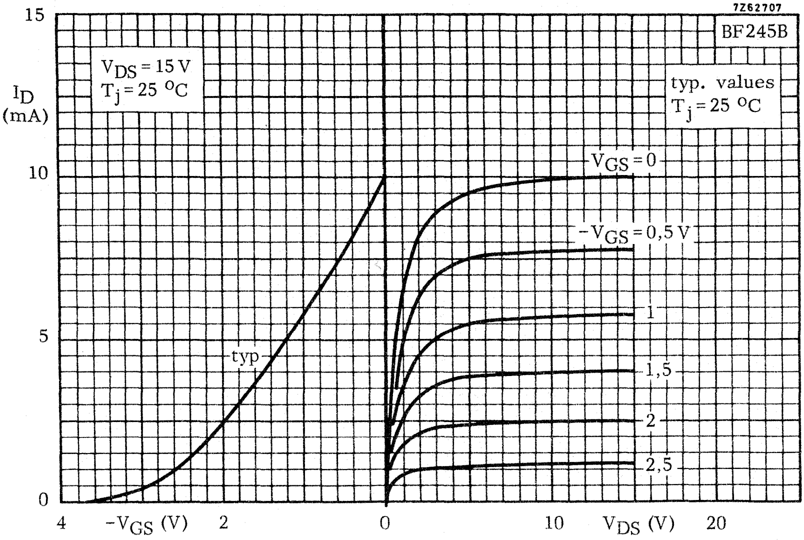
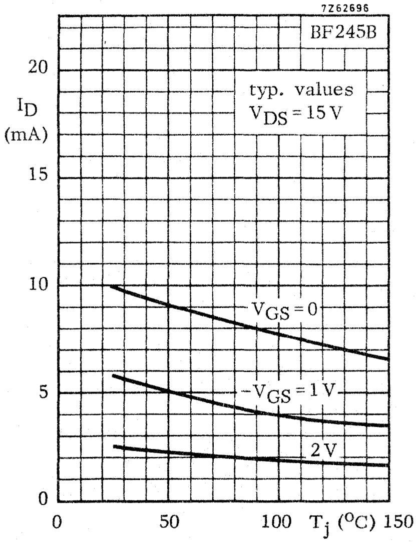
* The frequency at which g_{fs} is 0,7 of its value at 1 kHz.

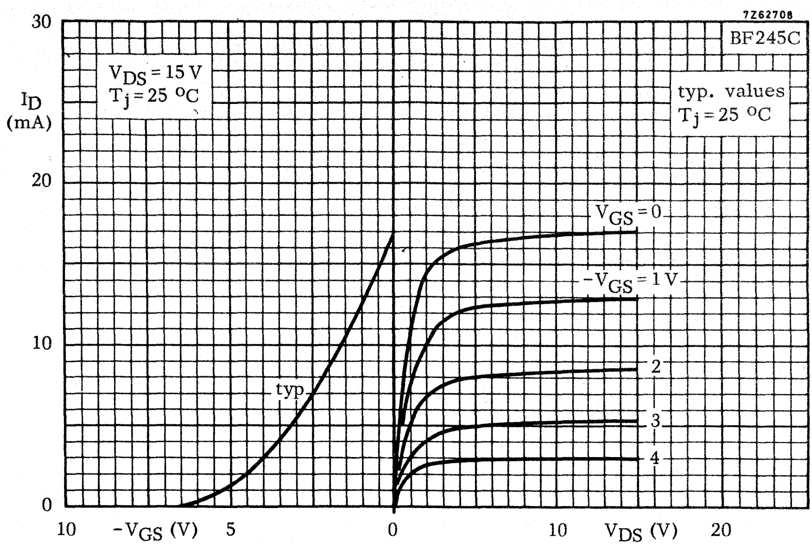

7Z62705
10
1
10^{-1}
10^{-2}
10^{-3}
$-I_{GSS}$ (nA)
$-V_{GS} = 20$ V
$V_{DS} = 0$
typ
0
50
100
T_j (°C)
150

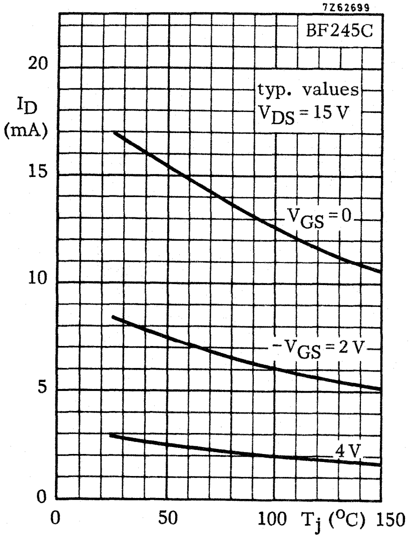

7Z62709
BF245A
6
4
2
0
I_D
(mA)
V_{DS} = 15 V
T_j = 25 °C
typ. values
T_j = 25 °C
V_{GS} = 0
$-V_{GS}$ = 0,5 V
1
1,5
typ
4
$-V_{GS}$ (V)
2
0
10
V_{DS} (V)
20

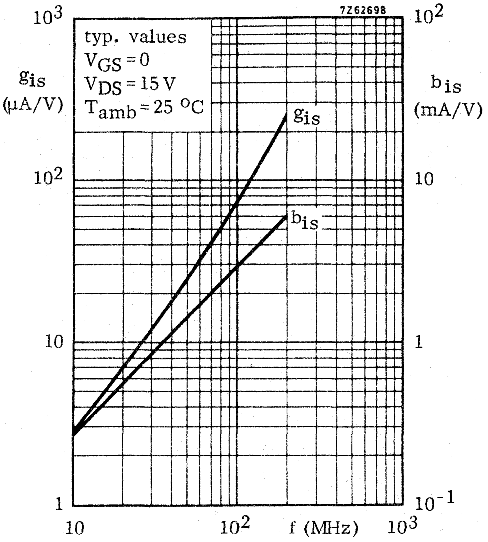

7Z62695
BF245A
4
3
2
1
0
I_D
(mA)
typ. values
V_{DS} = 15 V
V_{GS} = 0
$-V_{GS}$ = 0,5 V
1 V
1,5 V
0
50
100
T_j (°C)
150

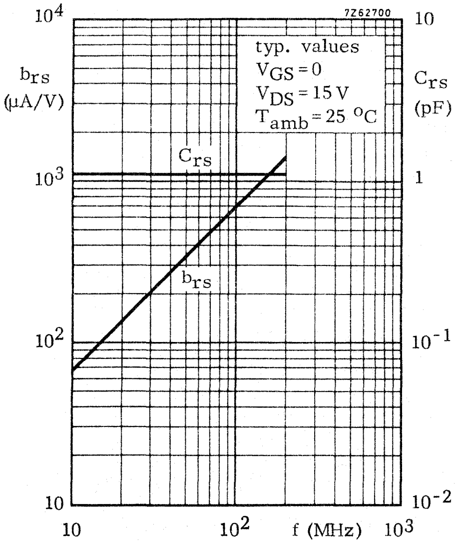

7Z62707
BF245B
V_{DS} = 15 V
T_j = 25 °C
typ. values
T_j = 25 °C
I_D (mA)
15
10
5
0
typ
V_{GS} = 0
$-V_{GS}$ = 0,5 V
1
1,5
2
2,5
4
$-V_{GS}$ (V)
2
0
10
V_{DS} (V)
20

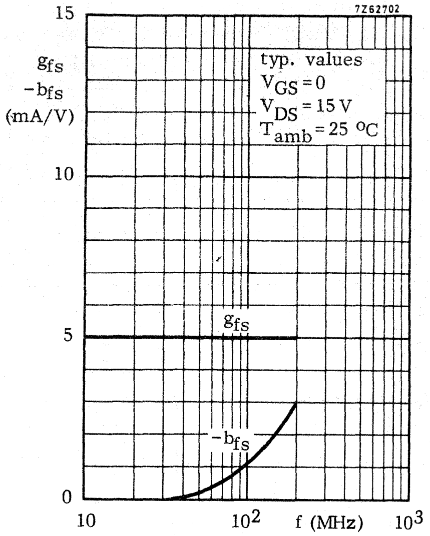

7Z62696
BF245B
typ. values
V_{DS} = 15 V
I_D (mA)
20
15
10
5
0
V_{GS} = 0
$-V_{GS}$ = 1 V
2 V
0
50
100
T_j (°C)
150

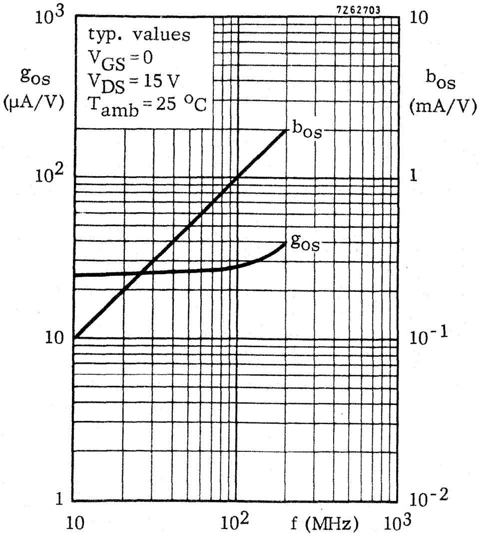

7Z62708
BF245C
V_{DS} = 15 V
T_j = 25 °C
typ. values
T_j = 25 °C
I_D (mA)
30
20
10
0
typ.
V_{GS} = 0
$-V_{GS}$ = 1 V
2
3
4
10
$-V_{GS}$ (V)
5
0
10
V_{DS} (V)
20

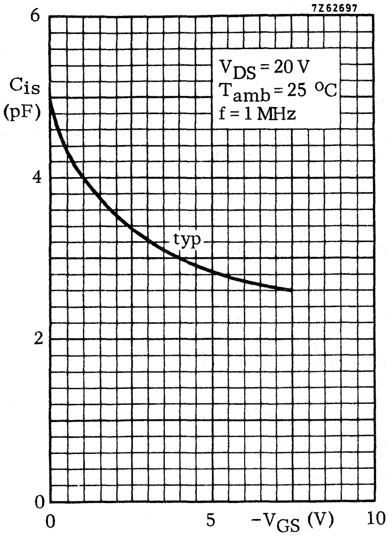

7Z62699
BF245C
typ. values
V_{DS} = 15 V
I_D (mA)
20
15
10
5
0
V_{GS} = 0
$-V_{GS}$ = 2 V
4 V
0
50
100
T_j (°C)
150

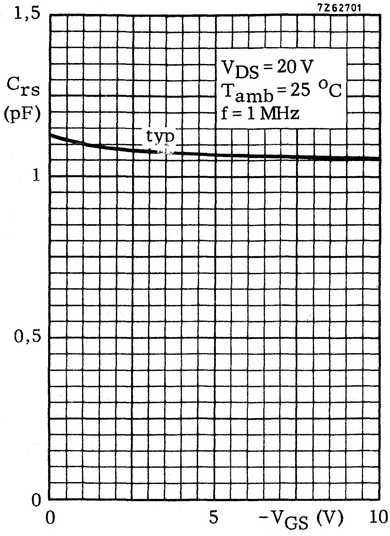

7Z62698
typ. values
$V_{GS} = 0$
$V_{DS} = 15$ V
$T_{amb} = 25$ °C
g_{is} (µA/V)
b_{is} (mA/V)
g_{is}
b_{is}
10^3
10^2
10
1
10^2
10
1
10^{-1}
10
10^2
f (MHz)
10^3

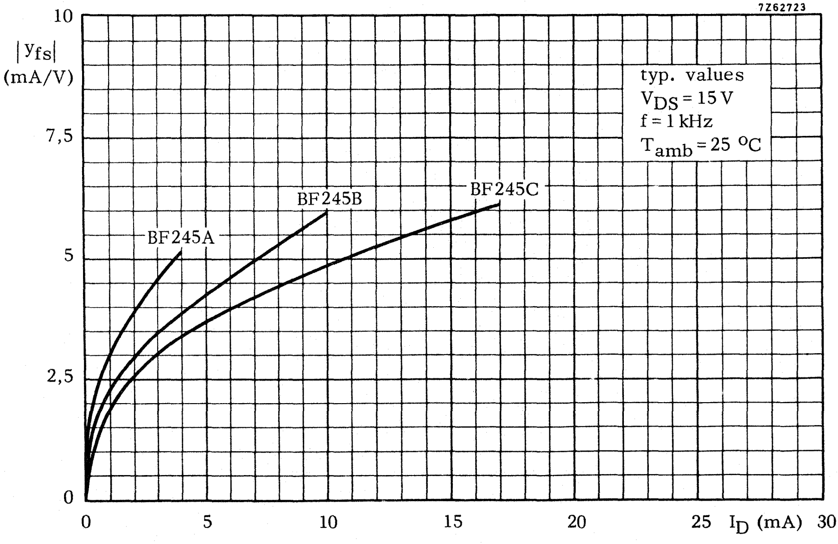

7Z62700
typ. values
$V_{GS} = 0$
$V_{DS} = 15$ V
$T_{amb} = 25$ °C
b_{rs} (µA/V)
C_{rs} (pF)
C_{rs}
b_{rs}
10^4
10^3
10^2
10
10
1
10^{-1}
10^{-2}
10
10^2
f (MHz)
10^3

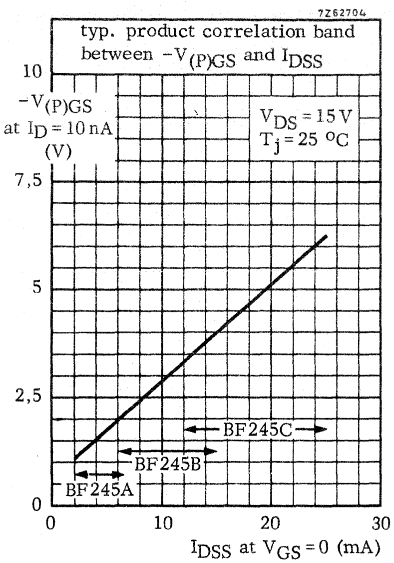

7Z62702
15
g_{fs}
$-b_{fs}$
(mA/V)
10
5
0
typ. values
$V_{GS} = 0$
$V_{DS} = 15$ V
$T_{amb} = 25$ °C
g_{fs}
$-b_{fs}$
10
10^2
f (MHz)
10^3

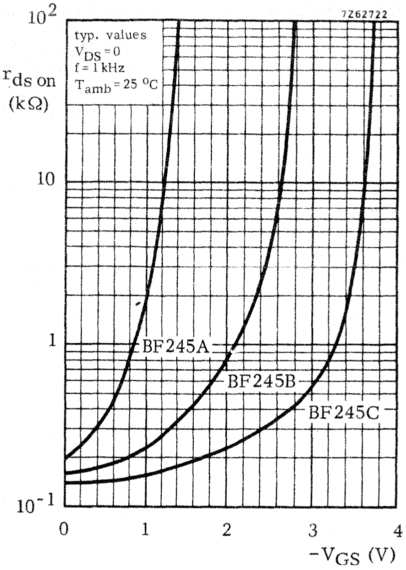

7Z62703
10^3
g_{os}
(μA/V)
10^2
10
1
10
b_{os}
(mA/V)
1
10^{-1}
10^{-2}
typ. values
$V_{GS} = 0$
$V_{DS} = 15$ V
$T_{amb} = 25$ °C
b_{os}
g_{os}
10
10^2
f (MHz)
10^3

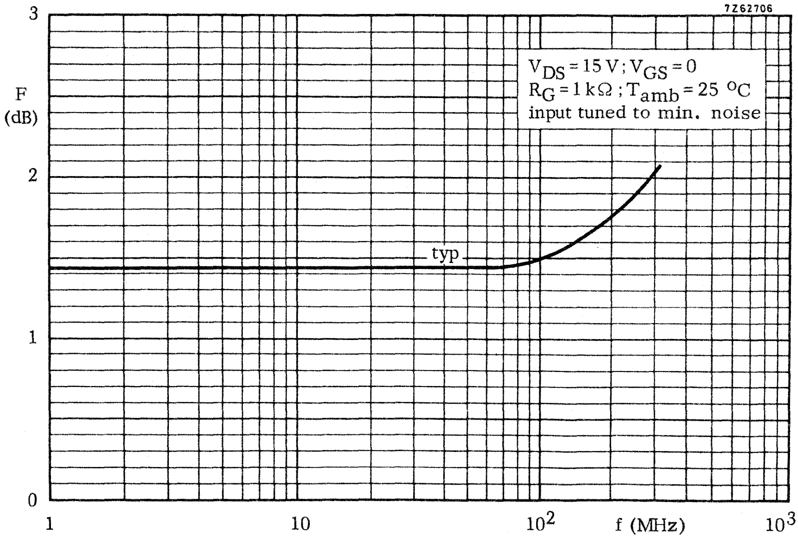

7Z62697
V_{DS} = 20 V
T_{amb} = 25 °C
f = 1 MHz
C_{is} (pF)
6
4
2
0
typ
0
5
$-V_{GS}$ (V)
10


7Z62701
V_{DS} = 20 V
T_{amb} = 25 °C
f = 1 MHz
C_{rs} (pF)
1,5
1
0,5
0
typ
0
5
$-V_{GS}$ (V)
10


7Z62723
$|y_{fs}|$ (mA/V)
10
7,5
5
2,5
0
typ. values
V_{DS} = 15 V
f = 1 kHz
T_{amb} = 25 °C
BF245A
BF245B
BF245C
0
5
10
15
20
25
I_D (mA)
30


7Z62704
typ. product correlation band
between $-V_{(P)GS}$ and I_{DSS}
$-V_{(P)GS}$
at $I_D = 10$ nA
(V)
$V_{DS} = 15$ V
$T_j = 25$ °C
10
7,5
5
2,5
0
BF245C
BF245B
BF245A
0
10
20
30
I_{DSS} at $V_{GS} = 0$ (mA)


7Z62722
10^2
typ. values
$V_{DS} = 0$
f = 1 kHz
$T_{amb} = 25$ °C
$r_{ds\,on}$
(kΩ)
10
1
10^{-1}
BF245A
BF245B
BF245C
0
1
2
3
4
$-V_{GS}$ (V)


7Z62706
3
2
1
0
F
(dB)
$V_{DS} = 15$ V; $V_{GS} = 0$
$R_G = 1$ kΩ; $T_{amb} = 25$ °C
input tuned to min. noise
typ
1
10
10^2
f (MHz)
10^3

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Symmetrical n-channel planar epitaxial junction field-effect transistors in plastic TO-92 variants, intended for v.h.f. and u.h.f. amplifiers, mixers, and general purpose switching.

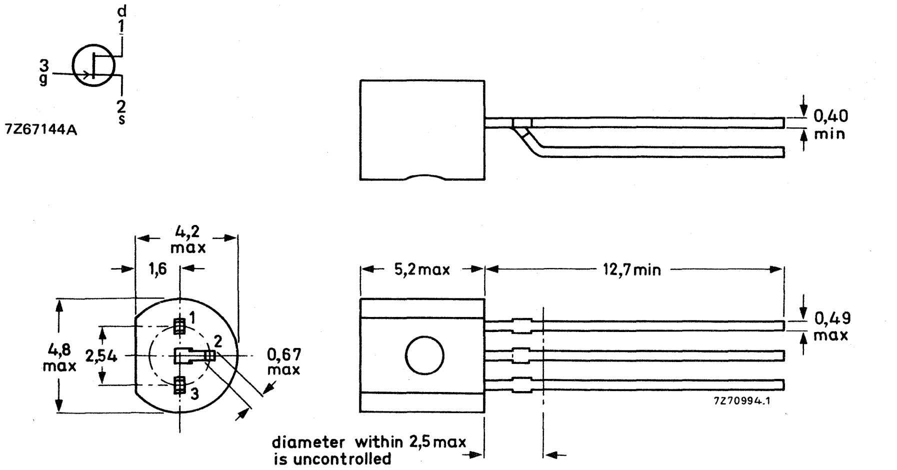
QUICK REFERENCE DATA

			BF247A	B	C	
Drain-source voltage	$\pm V_{DS}$	max.			25	V
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.			250	mW
Drain current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	30	60	110	mA
		<	80	140	250	mA
Gate-source cut-off voltage I_D = 10 nA; V_{DS} = 15 V	$-V_{(P)GS}$				0,6 to 14,5	V
Feedback capacitance at f = 1 MHz $I_D \leq$ 10 mA; V_{DS} = 15 V	C_{rs}	typ.			3,5	pF
Transfer admittance (common source) I_D = 10 mA; V_{DS} = 15 V; f = 1 kHz	$\lvert y_{fs} \rvert$	>			8	mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	25	V
Gate current	I_G	max.	10	mA
Total power dissipation up to $T_{amb} = 25\ ^{o}C$	P_{tot}	max.	250	mW
Storage temperature	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	500	K/W

CHARACTERISTICS

$T_{amb} = 25\ ^{o}C$

			BF247A	B	C	
Gate cut-off current $-V_{GS} = 15$ V; $V_{DS} = 0$	$-I_{GSS}$	<	5	5	5	nA
Drain current* $V_{DS} = 15$ V; $V_{GS} = 0$	I_{DSS}	>	30	60	110	mA
		<	80	140	250	mA
Gate-source breakdown voltage $-I_G = 1\ \mu A$; $V_{DS} = 0$	$-V_{(BR)GSS}$	>	25	25	25	V
Gate-source voltage $I_D = 200\ \mu A$; $V_{DS} = 15$ V	$-V_{GS}$	>	1,5	3,0	5,5	V
		<	4,0	7,0	12,0	V

Gate-source cut-off voltage $I_D = 10$ nA; $V_{DS} = 15$ V	$-V_{(P)GS}$		0,6 to 14,5	V
Transfer admittance (common source) $I_D = 10$ mA; $V_{DS} = 15$ V; f = 1 kHz	$\lvert y_{fs} \rvert$	>	8	mS
		typ.	17	mS
Capacitances at f = 1 MHz $I_D = 10$ mA; $V_{DS} = 15$ V				
feed-back capacitance	C_{rs}	typ.	3,5	pF
input capacitance	C_{is}	typ.	11	pF
output capacitance	C_{cs}	typ.	5	pF
Cut-off frequency** $V_{DS} = 15$ V; $V_{GS} = 0$	f_{gfs}	typ.	450	MHz

---

* Measured under pulse conditions; $t_p = 300\ \mu s$; $\delta \leqslant 0{,}02$.

** The frequency at which g_{fs} is 0,7 of its value at 1 kHz.

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Symmetrical N-channel planar epitaxial junction field-effect transistors in a plastic TO-92 variant; intended for v.h.f. and u.h.f. applications.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	300	mW

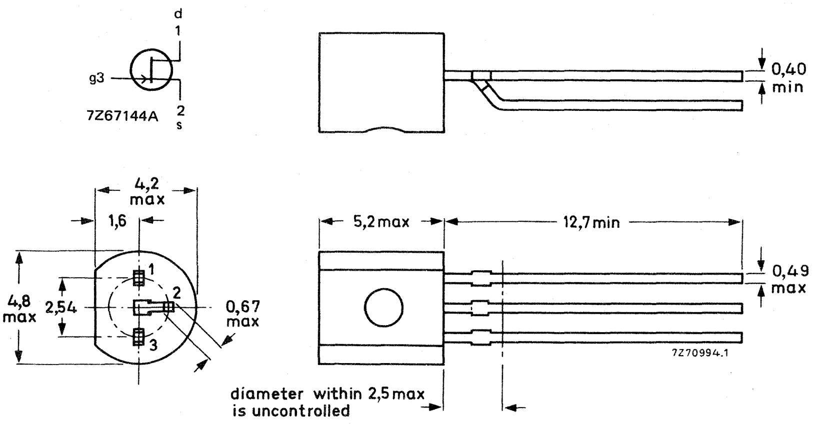
		BF256A	B	C	
Drain current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	$>$ 3	6	11	mA
		$<$ 7	13	18	mA

Feedback capacitance at f = 1 MHz V_{DS} = 20 V; $-V_{GS}$ = 1 V; T_{amb} = 25 °C	C_{rs}	typ.	0,7	pF
Transfer admittance (common source) V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz; T_{amb} = 25 °C	$\lvert y_{fs} \rvert$	$>$	4,5	mS
Power gain at f = 800 MHz V_{DS} = 15 V; R_S = 47 Ω	G_p	typ.	11	dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30 V
Drain-gate voltage (open source)	V_{DGO}	max.	30 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30 V
Gate current	I_G	max.	10 mA
Total power dissipation			
up to T_{amb} = 75 °C	P_{tot}	max.	300 mW
up to T_{amb} = 90 °C	P_{tot}	max.	300 mW 1)
Storage temperature	T_{stg}	−65 to + 150 °C	
Junction temperature	T_j	max.	150 °C

→ THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\,j\text{-}a}$	=	0,25 K/mW
From junction to ambient	$R_{th\,j\text{-}a}$	=	0,20 K/mW 1)

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

Gate cut-off current $-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	<	5 nA		

			BF256A	B	C	
Drain current 2) → V_{DS} = 15 V; V_{GS} = 0	I_{DSS} 3)	>	3	6	11	mA
		<	7	13	18	mA

Gate-source breakdown voltage $-I_G$ = 1 μA; V_{DS} = 0	$-V_{(BR)GSS}$	>	30 V
Gate-source voltage → I_D = 200 μA; V_{DS} = 15 V	$-V_{GS}$ 3)		0,5 to 7,5 V

---

1) Transistor mounted on printed circuit board, maximum lead length 3 mm, mounting pad for drain lead minimum 10 mm x 10 mm.

2) Measured under pulse conditions: t_p = 300 μs; $\delta \leqslant 0{,}02$.

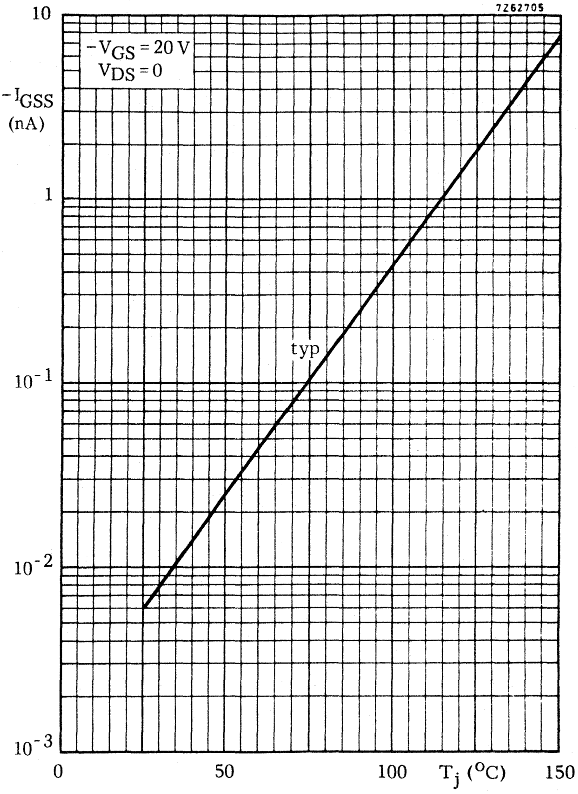
→ 3) BF256B/1: I_{DSS} = 6 to 8 mA; $-V_{GS}$ = 1,4 to 2,6 V.

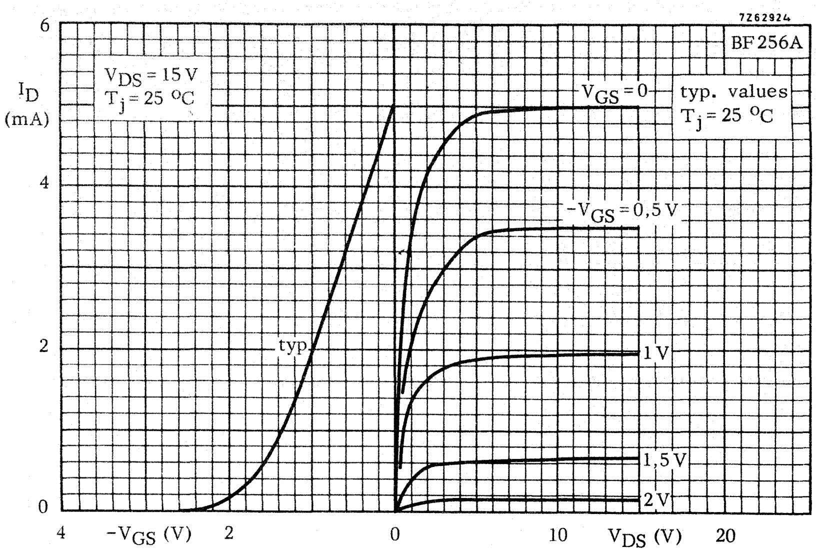
y-parameters (common source)				
Transistor admittance at f = 1 kHz V_{DS} = 15 V; V_{GS} = 0	$\lvert y_{fs} \rvert$	$>$	4,5 mS	1) ←
		typ.	5 mS	1)
Output capacitance at f = 1 MHz V_{DS} = 20 V; V_{GS} = 0	C_{os}	typ.	1,2 pF	
Feedback capacitance at f = 1 MHz V_{DS} = 20 V; $-V_{GS}$ = 1 V	C_{rs}	typ.	0,7 pF	
Cut-off frequency V_{DS} = 15 V; V_{GS} = 0	f_{gfs}	typ.	1 GHz	2)
Noise figure at f = 800 MHz V_{DS} = 10 V; R_S = 47 Ω	F	typ.	7,5 dB	
Power gain at f = 800 MHz V_{DS} = 15 V; R_S = 47 Ω	G_p	typ.	11 dB	

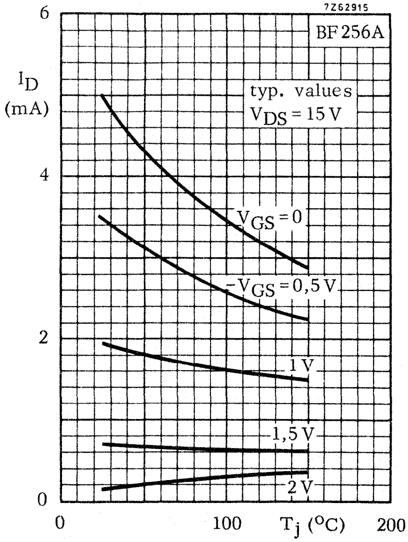
---

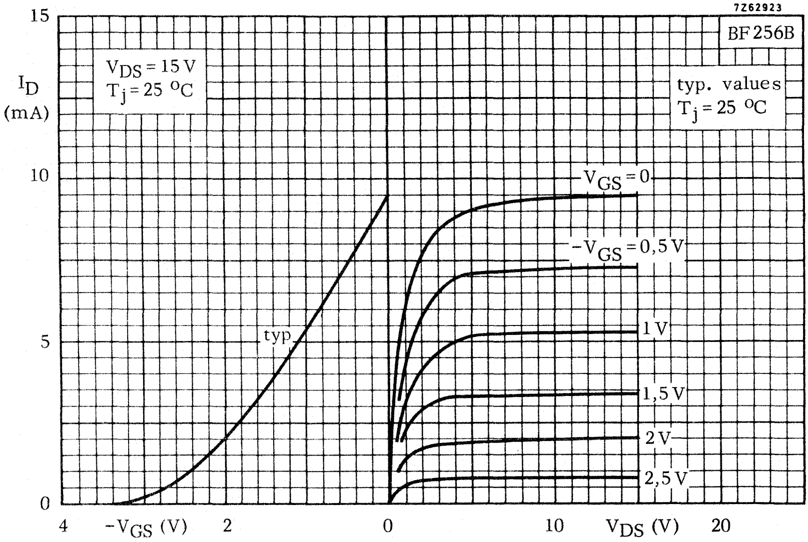
1) Measured under pulse conditions: $t_p = 300\ \mu s$; $\delta \leqslant 0{,}02$.

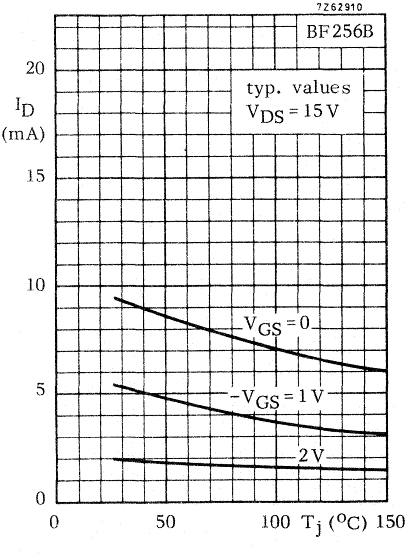
2) The frequency at which g_{fs} is 0,7 of its value at 1 kHz.

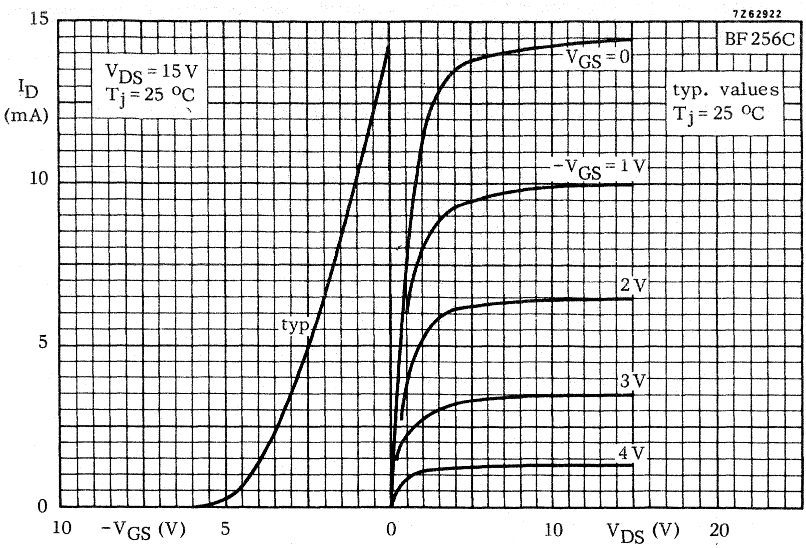

7Z62705
$-V_{GS}$ = 20 V
V_{DS} = 0
$-I_{GSS}$ (nA)
10
1
10^{-1}
10^{-2}
10^{-3}
typ
0
50
100
T_j (°C)
150

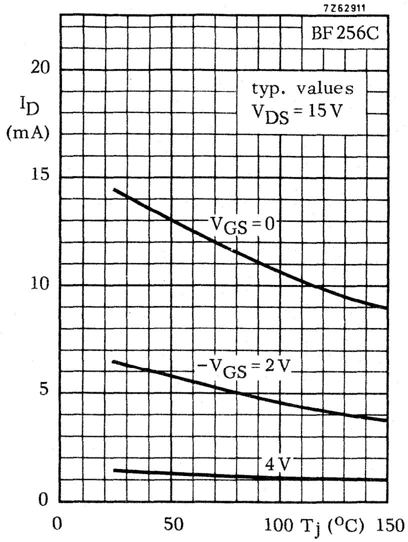

7Z62924
BF256A
I_D (mA)
6
4
2
0
V_{DS} = 15 V
T_j = 25 °C
typ.
V_{GS} = 0
typ. values
T_j = 25 °C
$-V_{GS}$ = 0,5 V
1 V
1,5 V
2 V
4
$-V_{GS}$ (V)
2
0
10
V_{DS} (V)
20

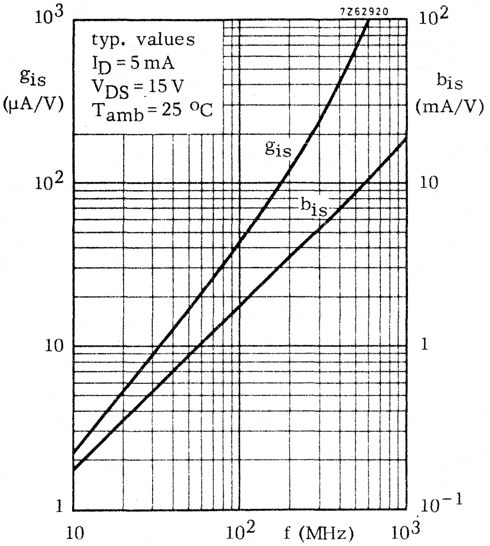

7Z62915
BF256A
I_D (mA)
6
4
2
0
typ. values
V_{DS} = 15 V
V_{GS} = 0
$-V_{GS}$ = 0,5 V
1 V
1,5 V
2 V
0
100
T_j (°C)
200

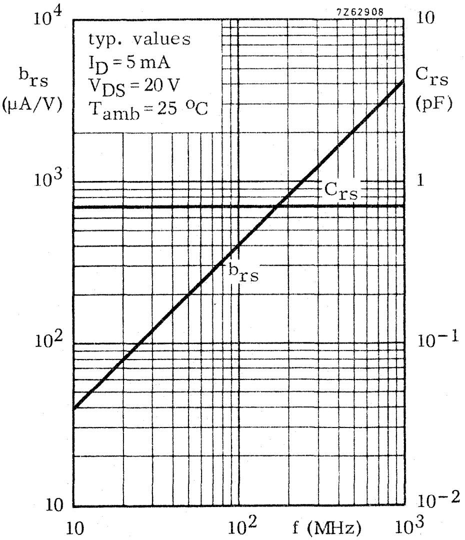

7Z62923
BF256B
15
10
5
0
I_D
(mA)
V_{DS} = 15 V
T_j = 25 °C
typ. values
T_j = 25 °C
typ
V_{GS} = 0
$-V_{GS}$ = 0,5 V
1 V
1,5 V
2 V
2,5 V
4
$-V_{GS}$ (V)
2
0
10
V_{DS} (V)
20

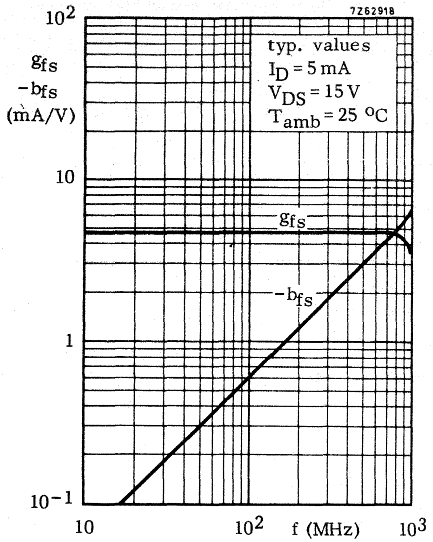

7Z62910
BF256B
typ. values
V_{DS} = 15 V
20
I_D
(mA)
15
10
5
0
V_{GS} = 0
$-V_{GS}$ = 1 V
2 V
0
50
100
T_j (°C)
150

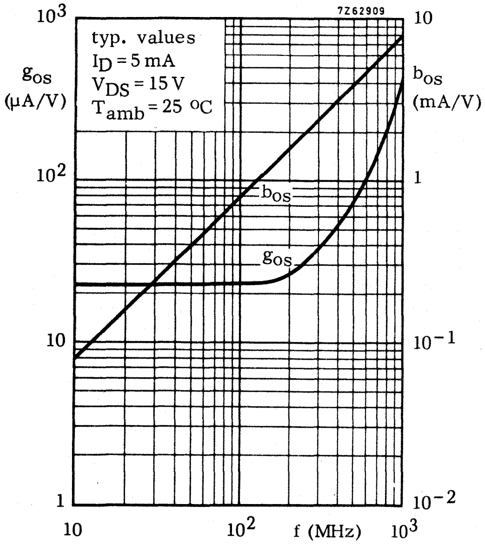

7Z62922
BF256C
V_{DS} = 15 V
T_j = 25 °C
I_D (mA)
15
10
5
0
typ. values
T_j = 25 °C
V_{GS} = 0
$-V_{GS}$ = 1 V
2 V
3 V
4 V
typ
10
$-V_{GS}$ (V)
5
0
10
V_{DS} (V)
20

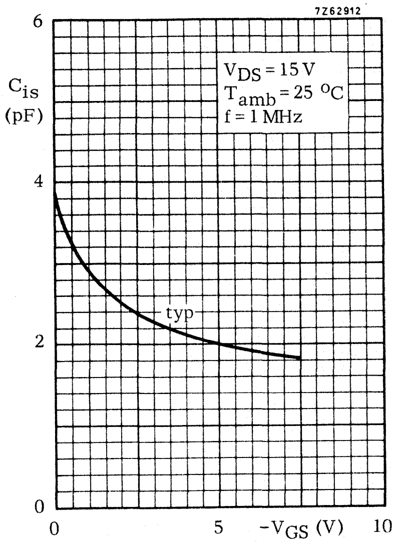

7Z62911
BF256C
typ. values
V_{DS} = 15 V
I_D (mA)
20
15
10
5
0
V_{GS} = 0
$-V_{GS}$ = 2 V
4 V
0
50
100 T_j (°C)
150

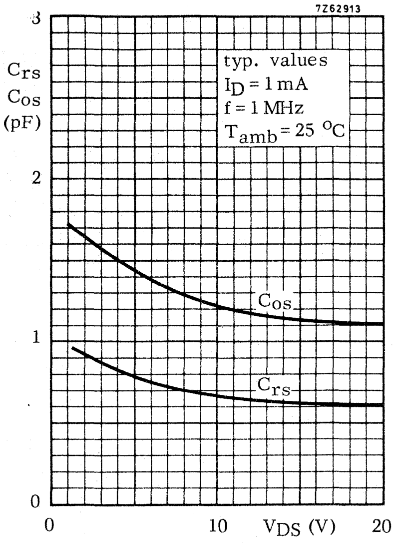

7Z62920
typ. values
I_D = 5 mA
V_{DS} = 15 V
T_{amb} = 25 °C
g_{is} (μA/V)
b_{is} (mA/V)
g_{is}
b_{is}
10^3
10^2
10
1
10^2
10
1
10^{-1}
10
10^2
f (MHz)
10^3

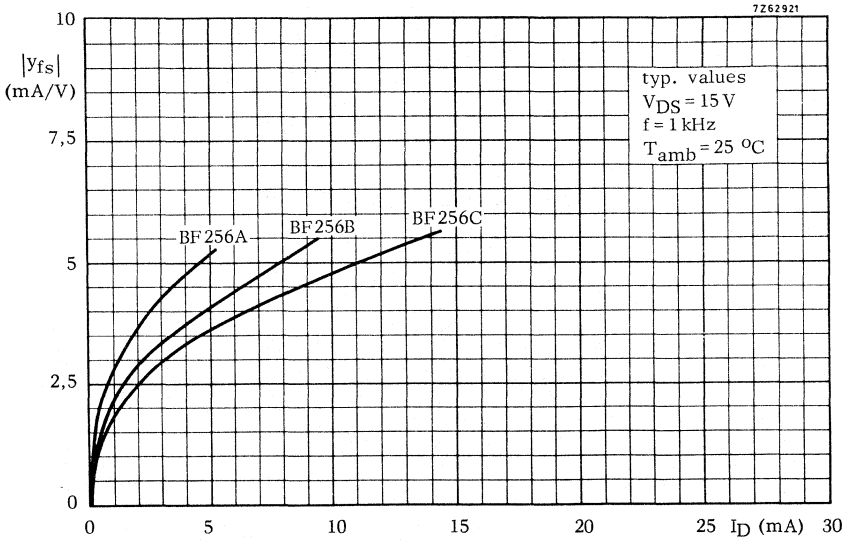

7Z62908
typ. values
I_D = 5 mA
V_{DS} = 20 V
T_{amb} = 25 °C
b_{rs} (μA/V)
C_{rs} (pF)
C_{rs}
b_{rs}
10^4
10^3
10^2
10
10
1
10^{-1}
10^{-2}
10
10^2
f (MHz)
10^3

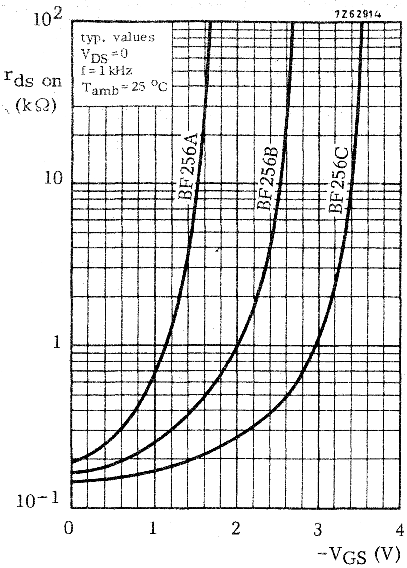

7Z62918
10^2
g_{fs}
$-b_{fs}$
(mA/V)
typ. values
$I_D = 5$ mA
$V_{DS} = 15$ V
$T_{amb} = 25$ °C
10
g_{fs}
$-b_{fs}$
1
10^{-1}
10
10^2
f (MHz)
10^3

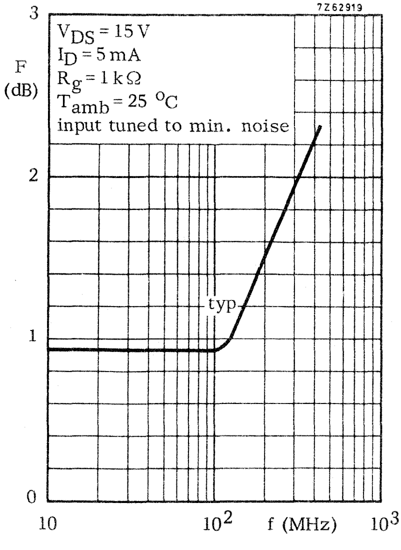

7Z62909
10^3
10
typ. values
$I_D = 5$ mA
$V_{DS} = 15$ V
$T_{amb} = 25$ °C
g_{os}
(μA/V)
b_{os}
(mA/V)
10^2
1
b_{os}
g_{os}
10
10^{-1}
1
10^{-2}
10
10^2
f (MHz)
10^3

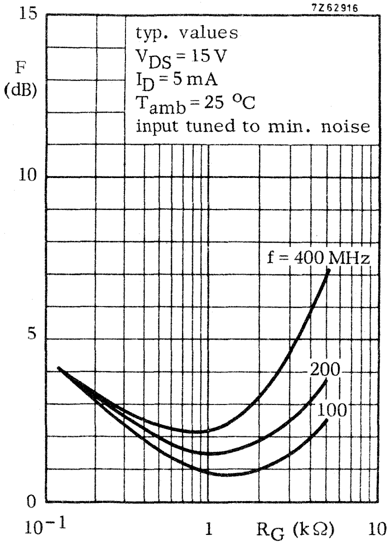

7Z62912
6
4
2
0
C_{is}
(pF)
V_{DS} = 15 V
T_{amb} = 25 °C
f = 1 MHz
typ
0
5
$-V_{GS}$ (V)
10


7Z62913
3
2
1
0
C_{rs}
C_{os}
(pF)
typ. values
I_D = 1 mA
f = 1 MHz
T_{amb} = 25 °C
C_{os}
C_{rs}
0
10
V_{DS} (V)
20


7Z62921
10
7,5
5
2,5
0
$|y_{fs}|$
(mA/V)
typ. values
V_{DS} = 15 V
f = 1 kHz
T_{amb} = 25 °C
BF256A
BF256B
BF256C
0
5
10
15
20
25
I_D (mA)
30


7Z62914
typ. values
$V_{DS} = 0$
f = 1 kHz
$T_{amb} = 25\ ^{\circ}C$
$r_{ds\ on}$ (kΩ)
10^2
10
1
10^{-1}
BF256A
BF256B
BF256C
0
1
2
3
4
$-V_{GS}$ (V)


7Z62919
$V_{DS} = 15$ V
$I_D = 5$ mA
$R_g = 1$ kΩ
$T_{amb} = 25\ ^{\circ}C$
input tuned to min. noise
F (dB)
3
2
1
0
typ
10
10^2
f (MHz)
10^3


7Z62916
typ. values
$V_{DS} = 15$ V
$I_D = 5$ mA
$T_{amb} = 25\ ^{\circ}C$
input tuned to min. noise
F (dB)
15
10
5
0
f = 400 MHz
200
100
10^{-1}
1
R_G (kΩ)
10

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Asymmetrical N-channel planar epitaxial junction field-effect transistors in a plastic TO-92 variant; intended for applications up to the v.h.f. range.

These FETs can be supplied in four I_{DSS} groups. Special features are the low feedback capacitance and the low noise figure. Thanks to these special features the BF410 is very suitable for applications such as the r.f. stages in f.m. portables (type A), car radios (type B) and mains radios (type C) or the mixer stage (type D).

QUICK REFERENCE DATA

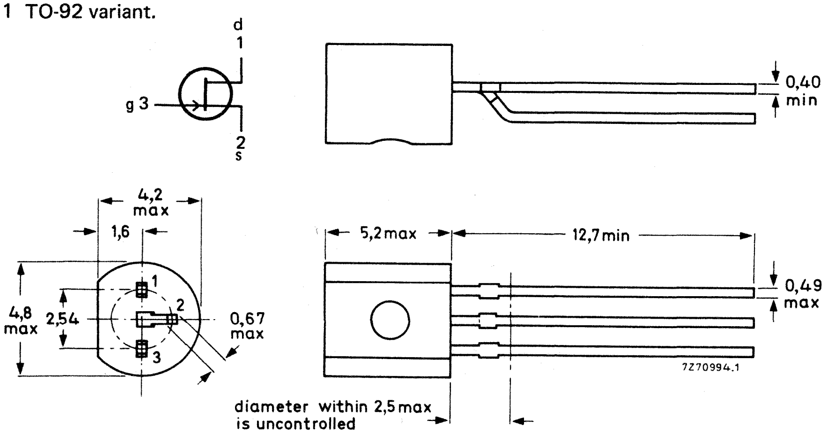
Drain-source voltage	V_{DS}	max.	20	V
Drain current (d.c. or average)	I_D	max.	30	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	300	mW

			BF410A	B	C	D	
Drain current V_{DS} = 10 V; V_{GS} = 0	I_{DSS}	$>$	0,7	2,5	6	10	mA
		$<$	3,0	7,0	12	18	mA
Transfer admittance (common source) V_{DS} = 10 V; V_{GS} = 0; f = 1 kHz	$\|y_{fs}\|$	$>$	2,5	4	6	7	mA/V
Feedback capacitance V_{DS} = 10 V; V_{GS} = 0	C_{rs}	typ.	0,3	0,3	–	–	pF
V_{DS} = 10 V; I_D = 5 mA	C_{rs}	typ.	–	–	0,3	0,3	pF
Noise figure at optimum source admittance G_S = 1 mA/V; $-B_S$ = 3 mA/V; f = 100 MHz V_{DS} = 10 V; V_{GS} = 0	F	typ.	1,5	1,5	–	–	dB
V_{DS} = 10 V; I_D = 5 mA	F	typ.	–	–	1,5	1,5	dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain-gate voltage (open source)	V_{DGO}	max.	20	V
Drain current (d.c. or average)	I_D	max.	30	mA
Gate current	$\pm I_G$	max.	10	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	300	mW
Storage temperature	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	0,25	°C/mW

STATIC CHARACTERISTICS

T_{amb} = 25 °C

			BF410A	B	C	D	
Gate cut-off current $-V_{GS}$ = 0,2 V; V_{DS} = 0	$-I_{GSS}$	<	10	10	10	10	nA
Gate-drain breakdown voltage I_S = 0; $-I_D$ = 10 µA	$-V_{(BR)GDO}$	>	20	20	20	20	V
Drain current V_{DS} = 10 V; V_{GS} = 0	I_{DSS}	>	0,7	2,5	6	10	mA
		<	3,0	7,0	12	18	mA
Gate-source cut-off voltage I_D = 10 µA; V_{DS} = 10 V	$-V_{(P)GS}$	typ.	0,8	1,5	2,2	3	V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): V_{DS} = 10 V; V_{GS} = 0; T_{amb} = 25 °C for **BF410A** and **B**
V_{DS} = 10 V; I_D = 5 mA; T_{amb} = 25 °C for **BF410C** and **D**

y-parameters (common source)			BF410A	B	C	D	
Input capacitance at f = 1 MHz	C_{is}	<	5	5	5	5	pF
Input conductance at f = 100 MHz	g_{is}	typ.	100	90	60	50	µA/V
Feedback capacitance at f = 1 MHz	C_{rs}	typ. <</br>	0,3 0,4	0,3 0,4	0,3 0,4	0,3 0,4	pF pF
Transfer admittance at f = 1 kHz	$\|y_{fs}\|$	>	2,5	4,0	4,0	3,5	mA/V
V_{GS} = 0 instead of I_D = 5 mA	$\|y_{fs}\|$	>	–	–	6,0	7,0	mA/V
Transfer admittance at f = 100 MHz	$\|y_{fs}\|$	typ.	3,5	5,5	5,0	5,0	mA/V
Output capacitance at f = 1 MHz	C_{os}	<	3	3	3	3	pF
Output conductance at f = 1 MHz	g_{os}	<	60	80	100	120	µA/V
Output conductance at f = 100 MHz	g_{os}	typ.	35	55	70	90	µA/V
Noise figure at optimum source admittance G_S = 1 mA/V; $-B_S$ = 3 mA/V; f = 100 MHz	F	typ.	1,5	1,5	1,5	1,5	dB

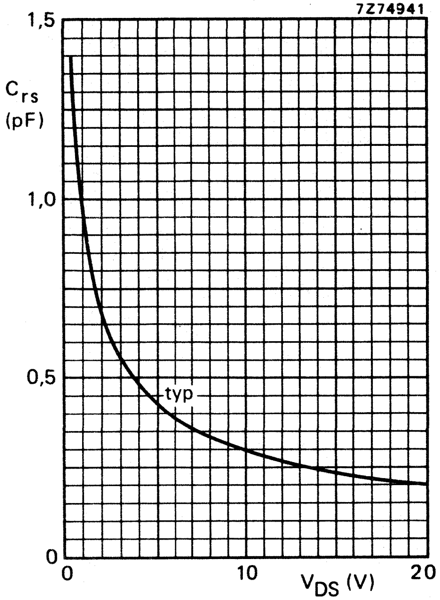


Fig. 2 $V_{GS} = 0$ for **BF410A** and **BF410B**; $I_D = 5$ mA for **BF410C** and **BF410D**; f = 1 MHz; $T_{amb} = 25$ °C.

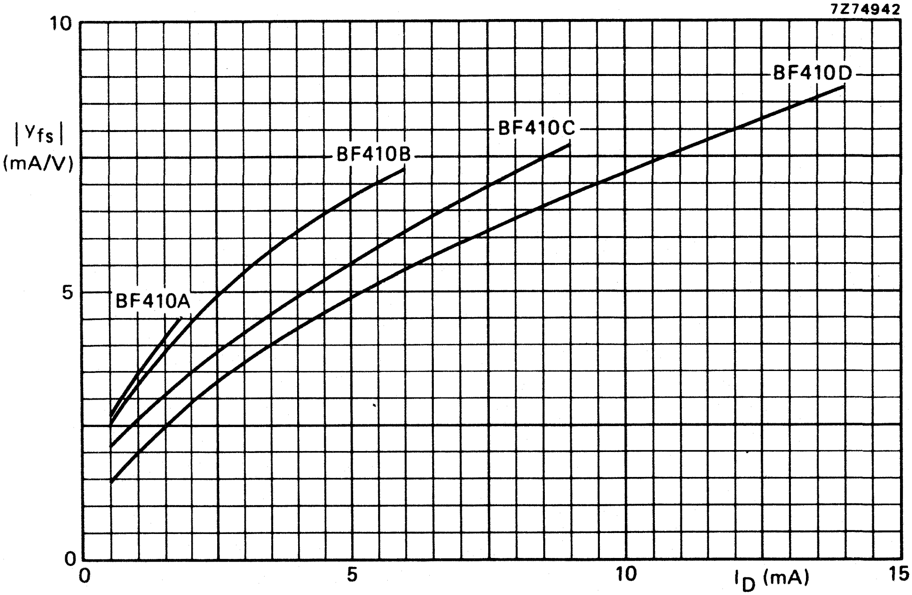


Fig. 3 $V_{DS} = 10$ V; f = 1 kHz; $T_{amb} = 25$ °C; typical values.

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Asymmetrical N-channel planar epitaxial junction field-effect transistors in the miniature plastic envelope intended for applications up to the v.h.f. range in hybrid thick and thin-film circuits. Special features are the low feedback capacitance and the low noise figure. These features make the product very suitable for applications such as the r.f. stages in f.m. portables (BF510), car radios (BF511) and mains radios (BF512) or the mixer stage (BF513).

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20				V
Drain current (d.c. or average)	I_D	max.	30				mA
Total power dissipation up to T_{amb} = 65 °C	P_{tot}	max.	250				mW
			BF510	511	512	513	
Drain current V_{DS} = 10 V; V_{GS} = 0	I_{DSS}	>	0,7	2,5	6	10	mA
		<	3,0	7,0	12	18	mA
Transfer admittance (common source) V_{DS} = 10 V; V_{GS} = 0; f = 1 kHz	$\|y_{fs}\|$	>	2,5	4	6	7	mA/V
Feedback capacitance V_{DS} = 10 V; V_{GS} = 0	C_{rs}	typ.	0,3	0,3	–	–	pF
V_{DS} = 10 V; I_D = 5 mA	C_{rs}	typ.	–	–	0,3	0,3	pF
Noise figure at optimum source admittance G_S = 1 mA/V; $-B_S$ = 3 mA/V; f = 100 MHz							
V_{DS} = 10 V; V_{GS} = 0	F	typ.	1,5	1,5	–	–	dB
V_{DS} = 10 V; I_D = 5 mA	F	typ.	–	–	1,5	1,5	dB

MECHANICAL DATA

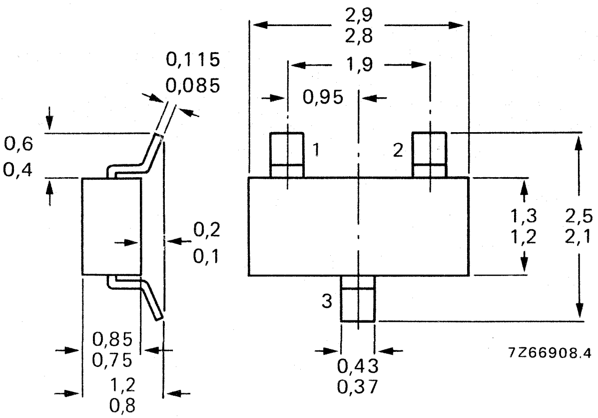
SOT-23

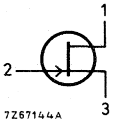
See also *Soldering recommendations.*

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-23





Marking code

BF510 = S6
BF511 = S7
BF512 = S8
BF513 = S9

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage see Fig. 4	V_{DS}	max.	20	V
Drain-gate voltage (open source) see Fig. 4	V_{DGO}	max.	20	V
Drain current (d.c. or average)	I_D	max.	30	mA
Gate current	$\pm I_G$	max.	10	mA
Total power dissipation up to T_{amb} = 60 °C**	P_{tot}	max.	250	mW
Storage temperature	T_{stg}	−65 to + 175		°C
Junction temperature	T_j	max.	175	°C

THERMAL CHARACTERISTICS*

$T_j = P x (R_{th\ j\text{-}t} + R_{th\ t\text{-}s} + R_{th\ s\text{-}a}) + T_{amb}$

Thermal resistance

From junction to tab	$R_{th\ j\text{-}t}$	=	60	K/W
From tab to soldering points	$R_{th\ t\text{-}s}$	=	280	K/W
From soldering points to ambient**	$R_{th\ s\text{-}a}$	=	90	K/W

---

* See *Thermal characteristics* in chapter GENERAL.

** Mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

STATIC CHARACTERISTICS

T_{amb} = 25 °C

			BF510	511	512	513	
Gate cut-off current $-V_{GS}$ = 0,2 V; V_{DS} = 0	$-I_{GSS}$	<	10	10	10	10	nA
Gate-drain breakdown voltage I_S = 0; $-I_D$ = 10 μA	$-V_{(BR)GDO}$	>	20	20	20	20	V
Drain current V_{DS} = 10 V; V_{GS} = 0	I_{DSS}	>	0,7	2,5	6	10	mA
		<	3,0	7,0	12	18	mA
Gate-source cut-off voltage I_D = 10 μA; V_{DS} = 10 V	$-V_{(P)GS}$	typ.	0,8	1,5	2,2	3	V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): V_{DS} = 10 V; V_{GS} = 0; T_{amb} = 25 °C for BF510 and BF511
V_{DS} = 10 V; I_D = 5 mA; T_{amb} = 25 °C for BF512 and BF513

y-parameters (common source)			BF510	511	512	513	
Input capacitance at f = 1 MHz	C_{is}	<	5	5	5	5	pF
Input conductance at f = 100 MHz	g_{is}	typ.	100	90	60	50	μA/V
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	0,3	0,3	0,3	0,3	pF
		<	0,4	0,4	0,4	0,4	pF
Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	>	2,5	4,0	4,0	3,5	mA/V
V_{GS} = 0 instead of I_D = 5 mA	$\lvert y_{fs} \rvert$	>	–	–	6,0	7,0	mA/V
Transfer admittance at f = 100 MHz	$\lvert y_{fs} \rvert$	typ.	3,5	5,5	5,0	5,0	mA/V
Output capacitance at f = 1 MHz	C_{os}	<	3	3	3	3	pF
Output conductance at f = 1 MHz	g_{os}	<	60	80	100	120	μA/V
Output conductance at f = 100 MHz	g_{os}	typ.	35	55	70	90	μA/V
Noise figure at optimum source admittance G_S = 1 mA/V; $-B_S$ = 3 mA/V; f = 100 MHz	F	typ.	1,5	1,5	1,5	1,5	dB

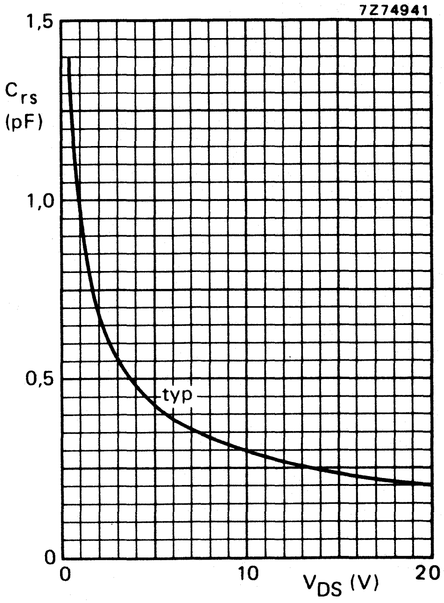


Fig. 2 $V_{GS} = 0$ for BF510 and BF511; $I_D = 5$ mA for BF512 and BF513; f = 1 MHz; $T_{amb} = 25\ ^oC$.

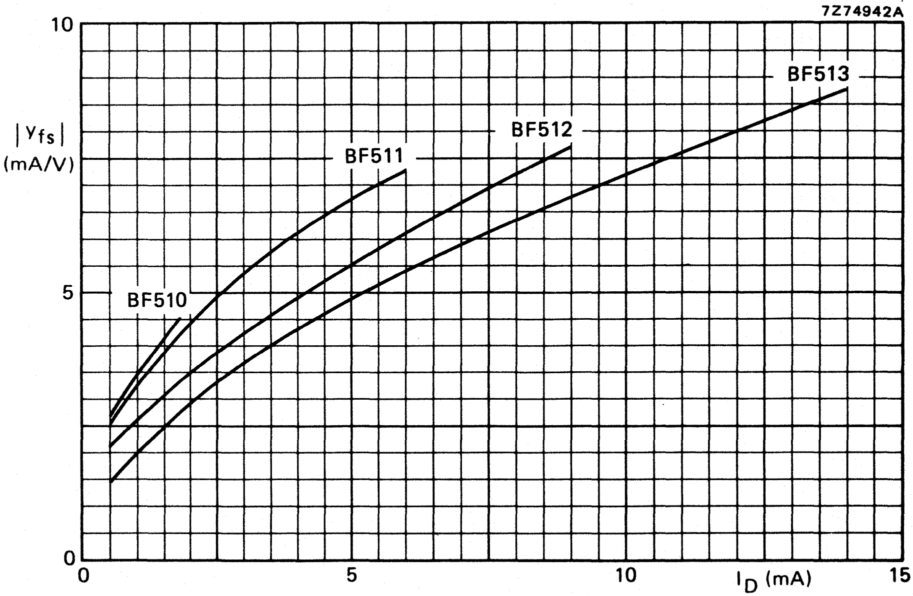


Fig. 3 $V_{DS} = 10$ V; f = 1 kHz; $T_{amb} = 25\ ^oC$; typical values.

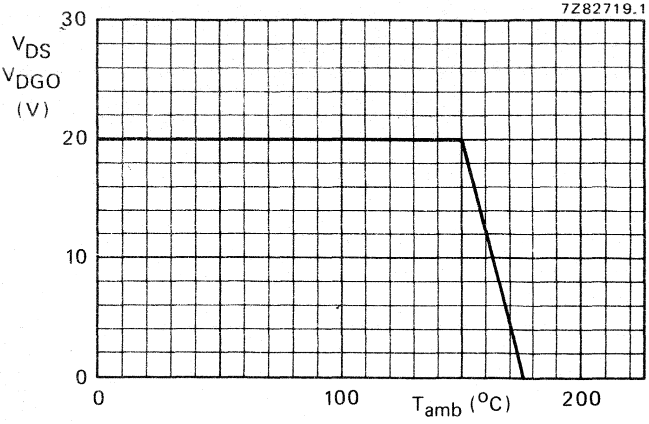


Fig. 4 Voltage derating curve.

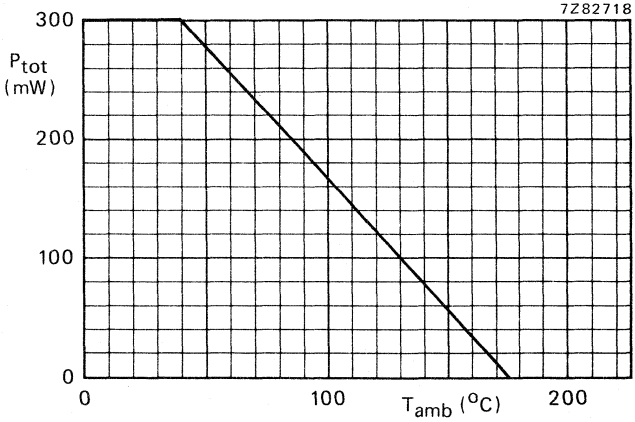


Fig. 5 Power derating curve.

DUAL N-CHANNEL FETS

Dual symmetrical n-channel silicon planar epitaxial junction field-effect transistors in a TO-71 metal envelope, with electrically insulated gates and a common substrate connected to the envelope; intended for high performance low level differential amplifiers.

QUICK REFERENCE DATA

Characteristics measured at T_{amb} = 25 °C; I_D = 200 μA; V_{DG} = 15 V

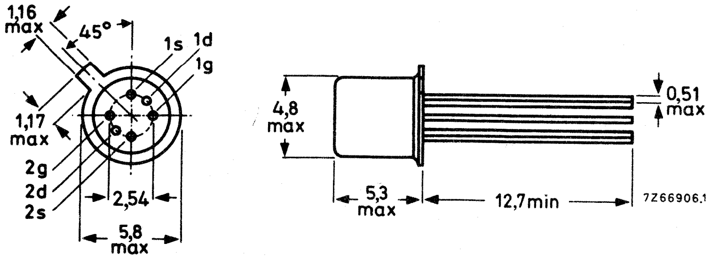
		BFQ10	11	12	13	14	15	16	
Difference in gate current	$\|\Delta I_G\|$	< 10	10	10	10	10	10	10	pA
Gate-source voltage difference	$\|\Delta V_{GS}\|$	< 5	10	10	10	15	20	50	mV
Thermal drift of gate-source voltage difference	$\left\|\frac{d\Delta V_{GS}}{dT}\right\|$	< 5	5	10	20	20	40	50	μV/K
Transfer conductance ratio	$\frac{g_{1fs}}{g_{2fs}}$	> 0,98 < 1,02	0,98 1,02	0,98 1,02	0,98 1,02	0,98 1,02	0,95 1,05	0,95 1,05	
Difference in transfer impedance	$\left\|\Delta \frac{1}{g_{fs}}\right\|$	< 6	6	12	12	12	20	30	Ω
Difference in penetration factor	$\left\|\Delta \frac{g_{os}}{g_{fs}}\right\|$	< 10	30	30	30	30	30	100	μV/V
Common mode rejection ratio	CMRR	> 100	90	90	90	90	90	80	dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-71.

All leads insulated from the case.



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages				
Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Voltage between gate 1 and gate 2	$\pm V_{1G-2G}$	max.	40	V
Currents				
Drain current	I_D	max.	30	mA
Gate current	I_G	max.	10	mA
Power dissipation				
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	250	mW
Temperatures				
Storage temperature	T_{stg}	-65 to +200		°C
Junction temperature	T_j	max.	200	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j-a}$	=	0,5	°C/mW

CHARACTERISTICS (total device) $T_{amb} = 25\ ^{o}C$ unless otherwise specified

Measured at: $I_D = 200\ \mu A$; $V_{DG} = 15\ V$ except for drain current ratio.

			BFQ10	11	12	13	14	15	16	
Drain current ratio [1] $V_{DG} = 15\ V$; $V_{GS} = 0$	$\frac{I_{1D-1SS}}{I_{2D-2SS}}$	>	0,97	0,95	0,95	0,95	0,92	0,90	0,80	
		<	1,03	1,05	1,05	1,05	1,08	1,10	1,20	
Difference in gate current	$\lvert \Delta I_G \rvert$	<	10	10	10	10	10	10	10	pA
Gate-source voltage difference	$\lvert \Delta V_{GS} \rvert$	<	5	10	10	10	15	20	50	mV
Thermal drift of gate-source voltage difference	$\left\lvert \frac{d\ \Delta V_{GS}}{dT} \right\rvert$	<	5	5	10	20	20	40	50	$\mu V/^{o}C$
Transfer conductance ratio	$\frac{g_{1fs}}{g_{2fs}}$	>	0,98	0,98	0,98	0,98	0,98	0,95	0,95	
		<	1,02	1,02	1,02	1,02	1,02	1,05	1,05	
Difference in transfer impedance [2]	$\left\lvert \Delta \frac{1}{g_{fs}} \right\rvert$	<	6	6	12	12	12	20	30	Ω
Difference in penetration factor [3]	$\left\lvert \Delta \frac{g_{os}}{g_{fs}} \right\rvert$	<	10	30	30	30	30	30	100	$\mu V/V$
Common mode rejection ratio [4]	CMRR	>	100	90	90	90	90	90	80	dB

---

[1] Measured under pulse conditions.

[2] The difference in transfer impedance is equal to the ratio of the change of the gate-source voltage difference to the change of drain current, at constant drain-gate voltage.
$(\Delta \frac{1}{g_{fs}} = \frac{d\ \Delta V_{GS}}{d\, I_D}$ at V_{DG} = constant)

[3] The difference in penetration factor is equal to the ratio of the change of the gate-source voltage difference to the change of drain-gate voltage, at constant drain current.
$(\Delta \frac{g_{os}}{g_{fs}} = \frac{d\ \Delta V_{GS}}{d\ V_{DG}}$ at I_D = constant)

[4] Common mode rejection ratio

$$\text{CMRR (in dB)} = -20 \log \left\lvert \Delta \frac{g_{os}}{g_{fs}} \right\rvert$$

CHARACTERISTICS (Individual transistor) T_{amb} = 25 °C unless otherwise specified

Gate cut-off current					
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	<	100	pA	
$-V_{GS}$ = 20 V; V_{DS} = 0; T_{amb} = 125 °C	$-I_{GSS}$	<	20	nA	
Gate current					
I_D = 200 μA; V_{DG} = 15 V; T_{amb} = 125 °C	I_G	<	10	nA	
Drain current					
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}		0,5 to 10	mA	1)
Gate-source voltage					
I_D = 200 μA; V_{DG} = 15 V	$-V_{GS}$	<	2,7	V	
Gate-source cut-off voltage					
I_D = 1 nA; V_{DG} = 15 V	$-V_{(P)GS}$		0,5 to 3,5	V	
Transfer conductance at f = 1 kHz					
I_D = 200 μA; V_{DG} = 15 V	g_{fs}	>	1,0	mA/V	
Output conductance at f = 1 kHz					
I_D = 200 μA; V_{DG} = 15 V	g_{os}	<	5	μA/V	
Input capacitance at f = 1 MHz					
I_D = 200 μA; V_{DG} = 15 V	C_{is}	<	8	pF	2)
Feedback capacitance at f = 1 MHz					
I_D = 200 μA; V_{DG} = 15 V	C_{rs}	<	1,0	pF	2)
Equivalent noise voltage					
I_D = 200 μA; V_{DS} = 15 V B = 0,6 to 100 Hz	V_n	<	0,5	μV	

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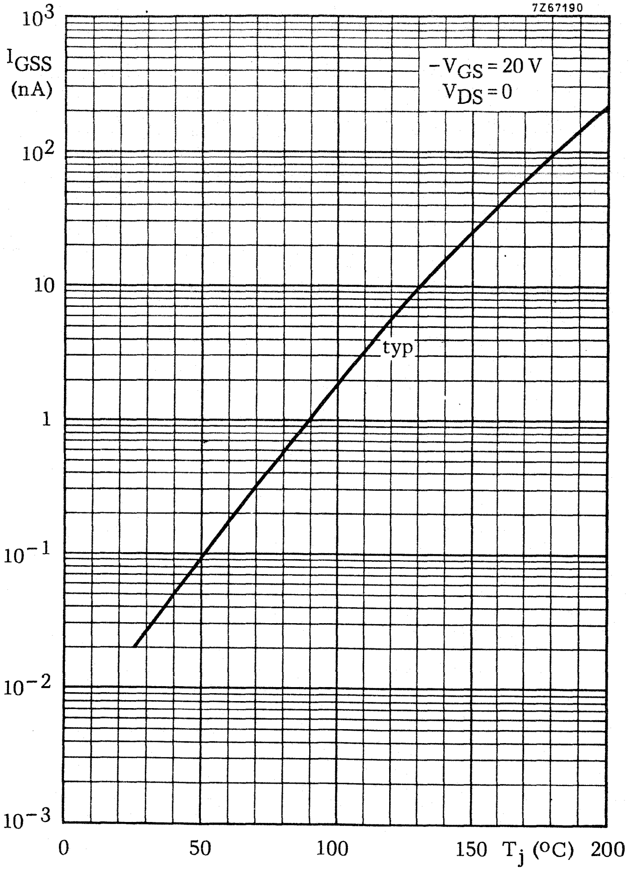
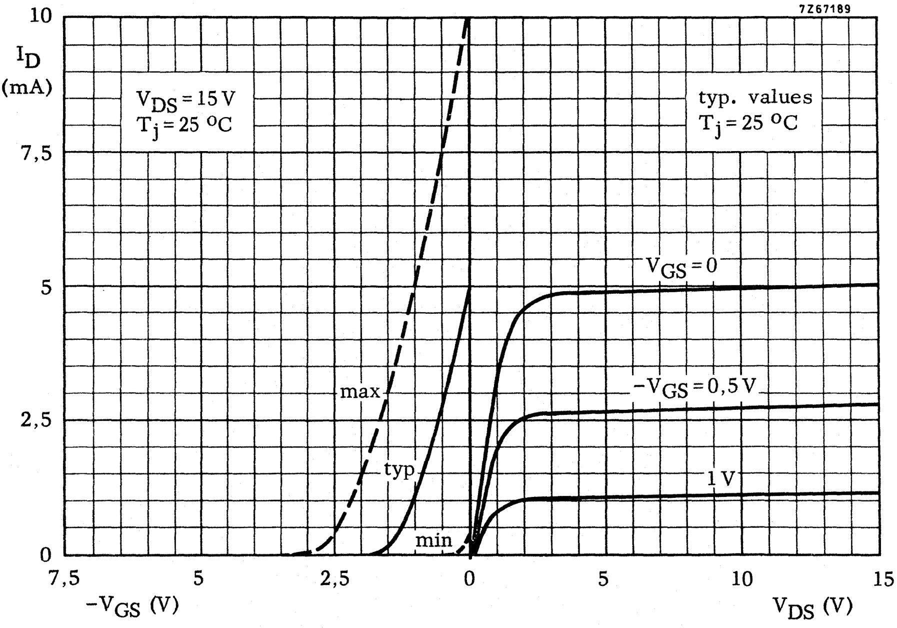
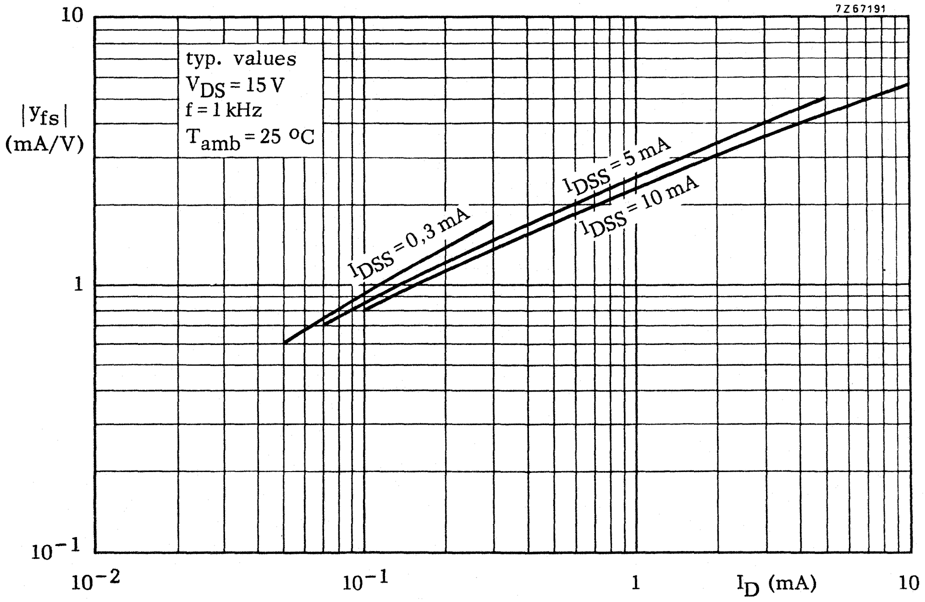
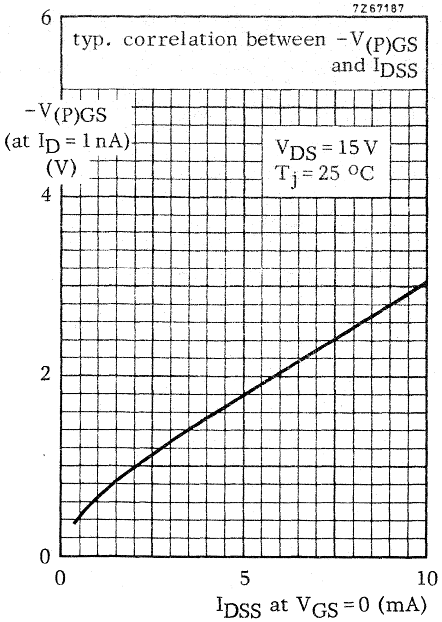
1) Measured under pulse conditions.

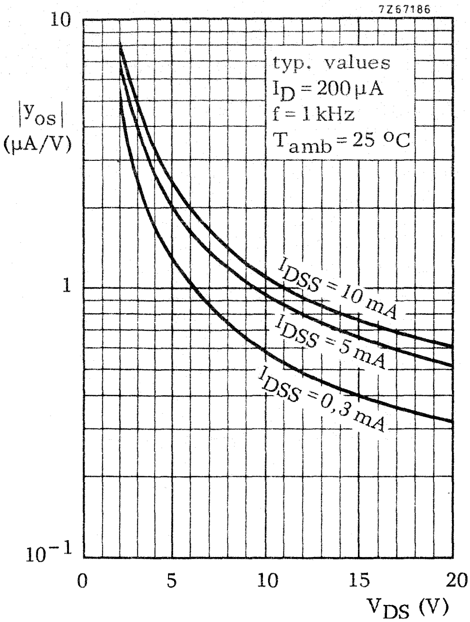
2) Measured with case grounded.

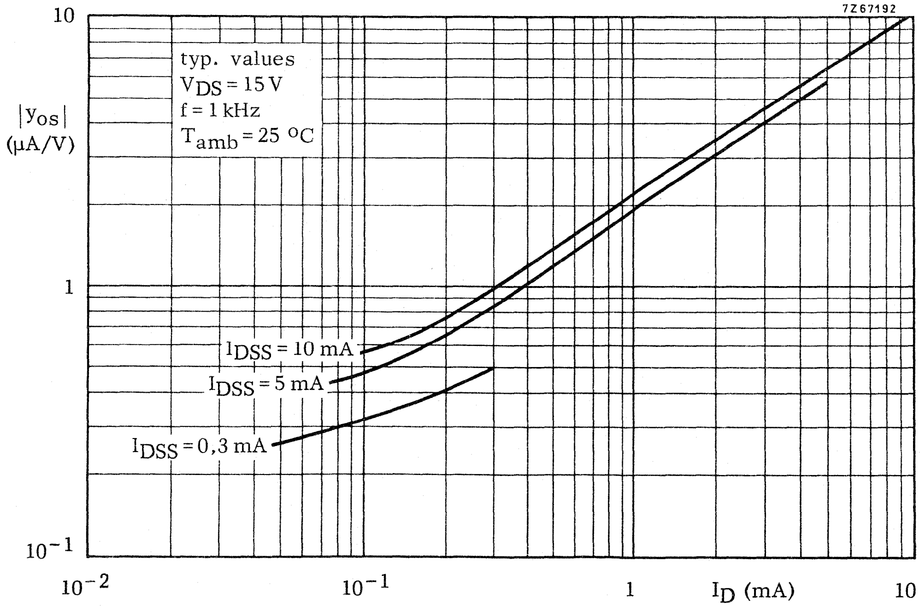

7Z67190
I_{GSS}
(nA)
10^3
10^2
10
1
10^{-1}
10^{-2}
10^{-3}
$-V_{GS} = 20$ V
$V_{DS} = 0$
typ
0
50
100
150
T_j (°C)
200

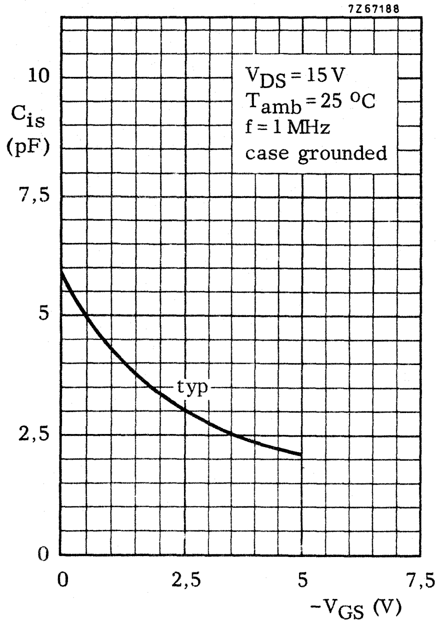

7Z67189
10
I_D
(mA)
7,5
5
2,5
0
V_DS = 15 V
T_j = 25 °C
typ. values
T_j = 25 °C
max
typ
min
V_GS = 0
−V_GS = 0,5 V
1 V
7,5
5
2,5
0
0
5
10
15
−V_GS (V)
V_DS (V)

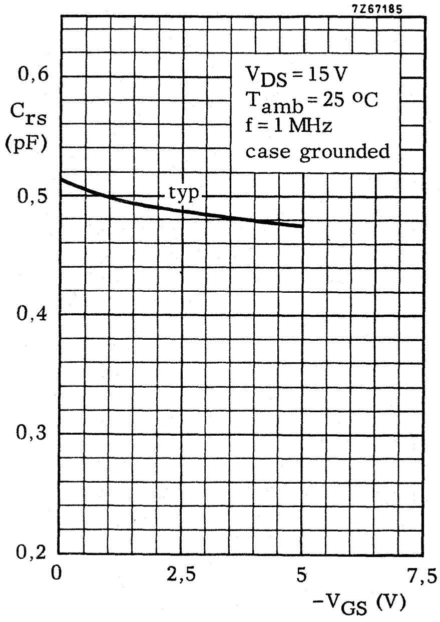

7Z67191
10
1
10⁻¹
|y_fs|
(mA/V)
typ. values
V_DS = 15 V
f = 1 kHz
T_amb = 25 °C
I_DSS = 0,3 mA
I_DSS = 5 mA
I_DSS = 10 mA
10⁻²
10⁻¹
1
I_D (mA)
10

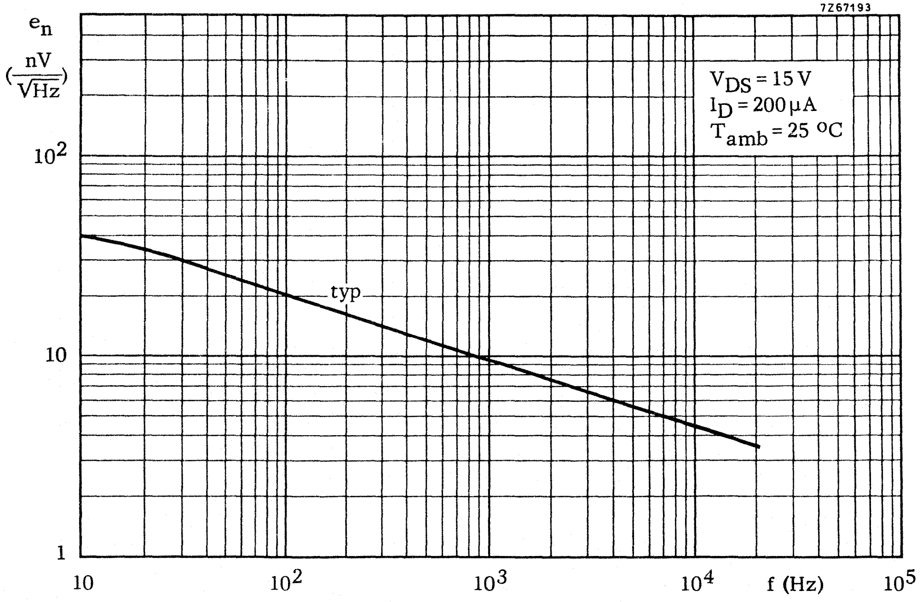

7Z67187
typ. correlation between $-V_{(P)GS}$ and I_{DSS}
$-V_{(P)GS}$ (at $I_D = 1$ nA) (V)
$V_{DS} = 15$ V
$T_j = 25$ °C
6
4
2
0
0
5
10
I_{DSS} at $V_{GS} = 0$ (mA)


7Z67186
typ. values
$I_D = 200$ µA
f = 1 kHz
$T_{amb} = 25$ °C
$|y_{os}|$ (µA/V)
10
1
10^{-1}
0
5
10
15
20
V_{DS} (V)
$I_{DSS} = 10$ mA
$I_{DSS} = 5$ mA
$I_{DSS} = 0{,}3$ mA


7Z67192
typ. values
$V_{DS} = 15$ V
f = 1 kHz
$T_{amb} = 25$ °C
$|y_{os}|$ (µA/V)
10
1
10^{-1}
10^{-2}
10^{-1}
1
I_D (mA)
10
$I_{DSS} = 10$ mA
$I_{DSS} = 5$ mA
$I_{DSS} = 0{,}3$ mA


7Z67188
C_{is} (pF)
10
7,5
5
2,5
0
V_{DS} = 15 V
T_{amb} = 25 °C
f = 1 MHz
case grounded
typ
0
2,5
5
7,5
$-V_{GS}$ (V)


7Z67185
C_{rs} (pF)
0,6
0,5
0,4
0,3
0,2
V_{DS} = 15 V
T_{amb} = 25 °C
f = 1 MHz
case grounded
typ
0
2,5
5
7,5
$-V_{GS}$ (V)


7Z67193
e_n $(\frac{nV}{\sqrt{Hz}})$
10^2
10
1
V_{DS} = 15 V
I_D = 200 µA
T_{amb} = 25 °C
typ
10
10^2
10^3
10^4
f (Hz)
10^5

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Planar epitaxial junction field effect transistor in a microminiature plastic envelope. It is intended for low level general purpose amplifiers in thick and thin-film circuits.

QUICK REFERENCE DATA

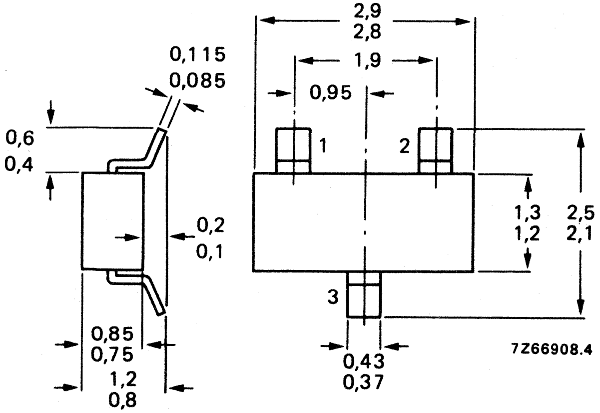
Drain-source voltage	$\pm V_{DS}$	max.	25		V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25		V
Total power dissipation up to $T_{amb} = 65\ ^oC$	P_{tot}	max.	250		mW
			BFR30	BFR31	
Drain current $V_{DS} = 10$ V; $V_{GS} = 0$	I_{DSS}	>	4	1	mA
		<	10	5	mA
Transfer admittance (common source) $I_D = 1$ mA; $V_{DS} = 10$ V; f = 1 kHz	$\lvert y_{fs} \rvert$	>	1,0	1,5	mA/V
		<	4,0	4,5	mA/V

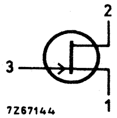
MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-23.

Marking code
BFR30 = M1
BFR31 = M2





See also *Soldering recommendations.*

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage see Fig. 2	$\pm V_{DS}$	max.	25	V
Drain-gate voltage (open source) see Fig. 2	V_{DGO}	max.	25	V
Gate-source voltage (open drain) see Fig. 2	$-V_{GSO}$	max.	25	V
Drain current	I_D	max.	10	mA
Gate current	I_G	max.	5	mA
Total power dissipation up to T_{amb} = 65 °C**	P_{tot}	max.	250	mW
Storage temperature	T_{stg}		−65 to + 175	°C
Junction temperature	T_j	max.	175	°C

THERMAL CHARACTERISTICS*

$T_j = P \times (R_{th\ j\text{-}t} + R_{th\ t\text{-}s} + R_{th\ s\text{-}a}) + T_{amb}$

Thermal resistance

From junction to tab	$R_{th\ j\text{-}t}$	=	60	K/W
From tab to soldering points	$R_{th\ t\text{-}s}$	=	280	K/W
From soldering points to ambient**	$R_{th\ s\text{-}a}$	=	90	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

			BFR30	BFR31	
Gate cut-off current $-V_{GS}$ = 10 V; V_{DS} = 0	$-I_{GSS}$	<	0,2	0,2	nA
Drain current V_{DS} = 10 V; V_{GS} = 0	I_{DSS}	>	4	1	mA
		<	10	5	mA
Gate-source voltage I_D = 1 mA; V_{DS} = 10 V	$-V_{GS}$	>	0,7	0	V
		<	3,0	1,3	V
I_D = 50 μA; V_{DS} = 10 V	$-V_{GS}$	<	4,0	2,0	V
Gate-source cut-off voltage I_D = 0,5 nA; V_{DS} = 10 V	$-V_{(P)GS}$	<	5	2,5	V
y parameters					
Transfer admittance at f = 1 kHz; T_{amb} = 25 °C I_D = 1 mA; V_{DS} = 10 V	$\lvert y_{fs} \rvert$	>	1,0	1,5	mA/V
		<	4,0	4,5	mA/V
I_D = 200 μA; V_{DS} = 10 V	$\lvert y_{fs} \rvert$	>	0,5	0,75	mA/V
Output admittance at f = 1 kHz I_D = 1 mA; V_{DS} = 10 V	$\lvert y_{os} \rvert$	<	40	25	μA/V
I_D = 200 μA; V_{DS} = 10 V	$\lvert y_{os} \rvert$	<	20	15	μA/V

---

* See *Thermal characteristics* in chapter GENERAL.

** Mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

y parameters (continued)

			BFR30	BFR31	
Input capacitance at f = 1 MHz					
I_D = 1 mA; V_{DS} = 10 V	C_{is}	<	4	4	pF
I_D = 200 μA; V_{DS} = 10 V	C_{is}	<	4	4	pF
Feedback capacitance at f = 1 MHz; T_{amb} = 25 °C					
I_D = 1 mA; V_{DS} = 10 V	C_{rs}	<	1,5	1,5	pF
I_D = 200 μA; V_{DS} = 10 V	C_{rs}	<	1,5	1,5	pF
Equivalent noise voltage					
I_D = 200 μA; V_{DS} = 10 V B = 0,6 to 100 Hz	V_n	<	0,5	0,5	μV

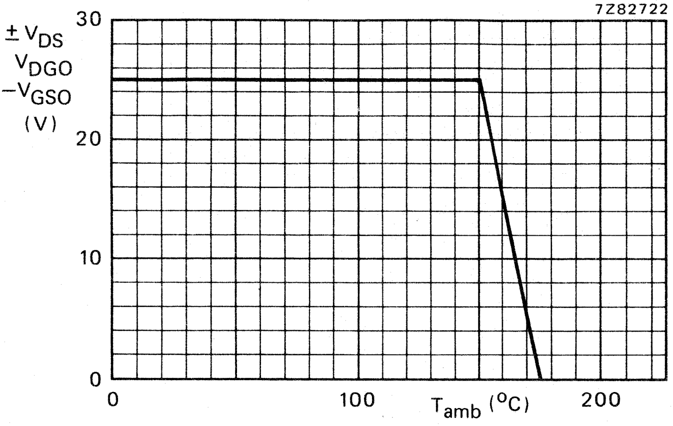


Fig. 2 Voltage derating curve.

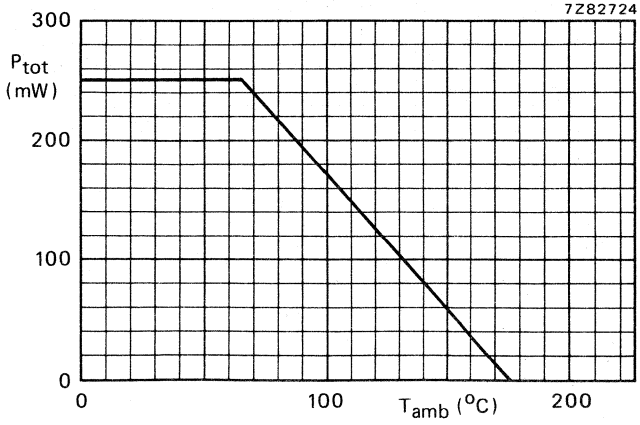


Fig. 3 Power derating curve.

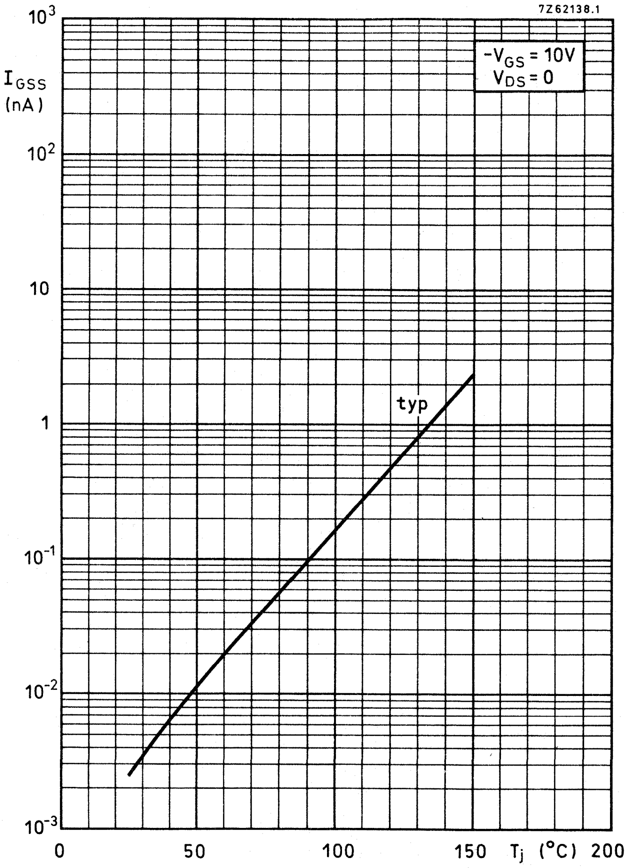

7Z62138.1
I_{GSS} (nA)
10^3
10^2
10
1
10^{-1}
10^{-2}
10^{-3}
$-V_{GS} = 10V$
$V_{DS} = 0$
typ
0
50
100
150
T_j (°C)
200

Fig. 4.

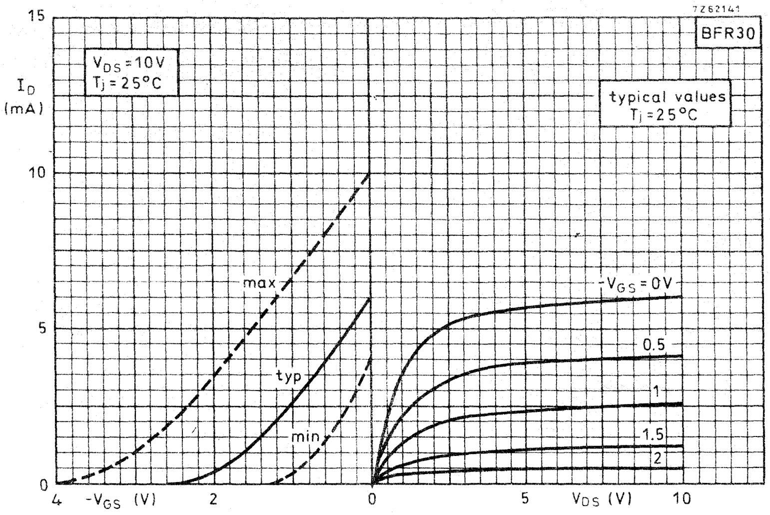

7Z62141
BFR30
15
10
5
0
I_D (mA)
V_DS = 10 V
Tj = 25 °C
typical values
Tj = 25 °C
max
typ
min
-V_GS = 0 V
0.5
1
1.5
2
4
-V_GS (V)
2
0
5
V_DS (V)
10

Fig. 5.

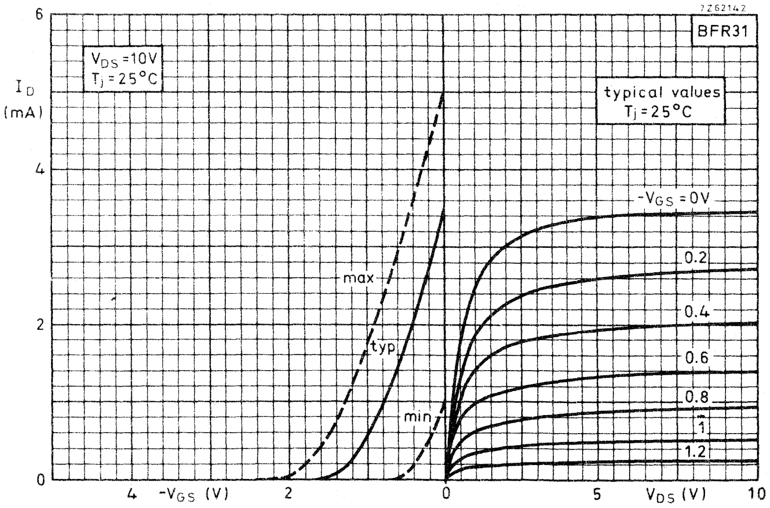

7Z62142
BFR31
6
4
2
0
I_D (mA)
V_DS = 10 V
Tj = 25 °C
typical values
Tj = 25 °C
max
typ
min
-V_GS = 0 V
0.2
0.4
0.6
0.8
1
1.2
4
-V_GS (V)
2
0
5
V_DS (V)
10

Fig. 6.

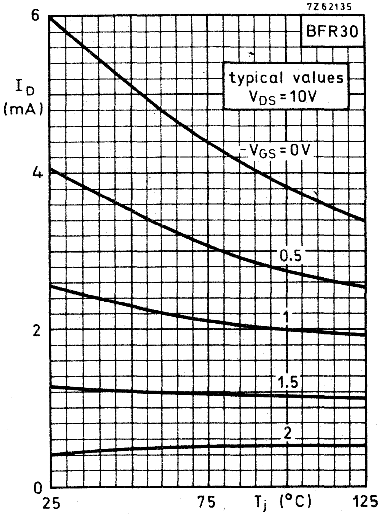


Fig. 7.

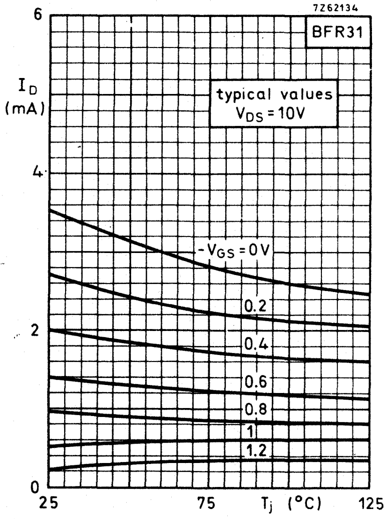


Fig. 8.

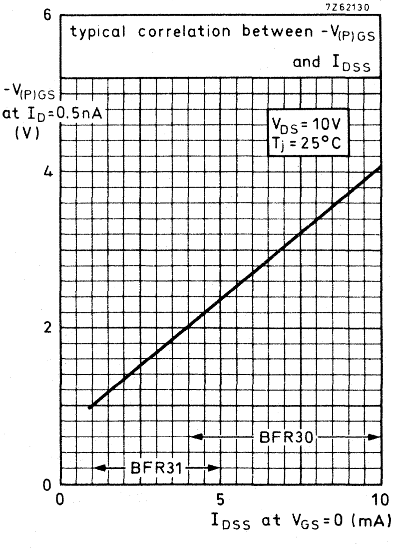


Fig. 9.

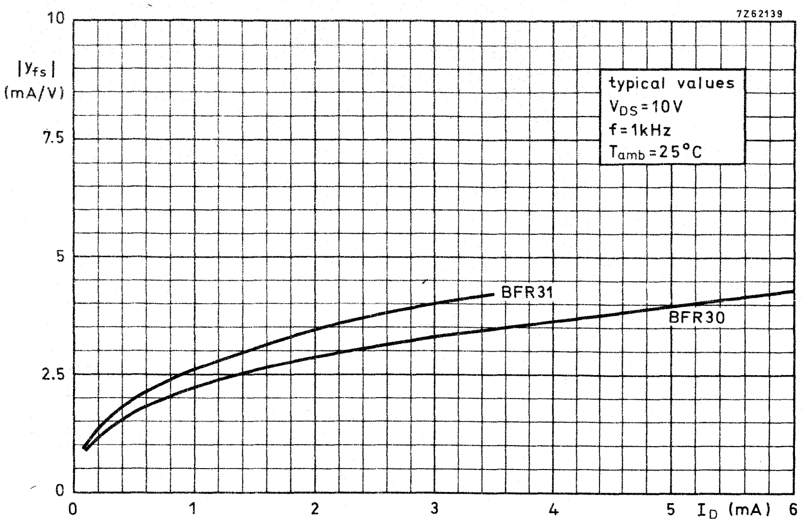

7Z62139
10
$|y_{fs}|$
(mA/V)
7.5
5
2.5
0
0
1
2
3
4
5
6
I_D (mA)
typical values
V_{DS} = 10 V
f = 1 kHz
T_{amb} = 25 °C
BFR31
BFR30

Fig. 10.

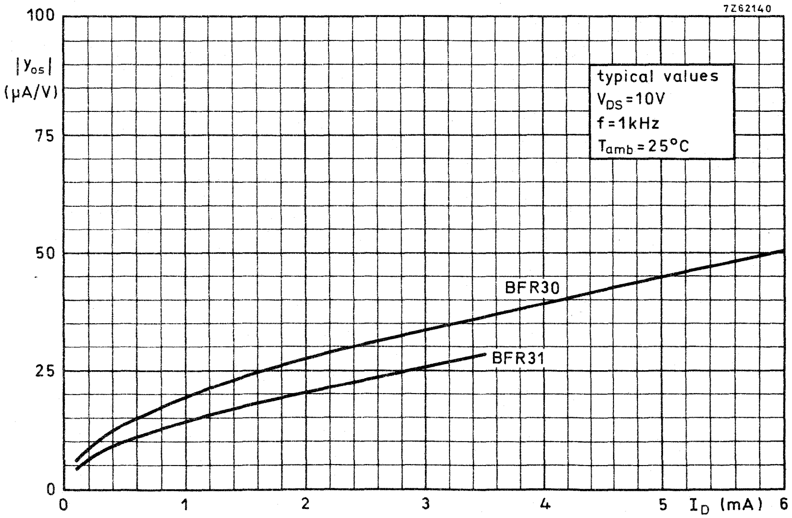

7Z62140
100
$|y_{os}|$
(μA/V)
75
50
25
0
0
1
2
3
4
5
6
I_D (mA)
typical values
V_{DS} = 10 V
f = 1 kHz
T_{amb} = 25 °C
BFR30
BFR31

Fig. 11.

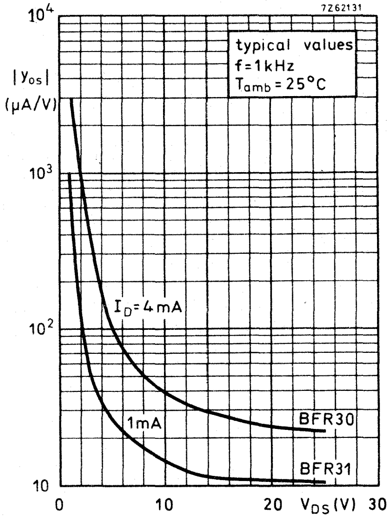


Fig. 12.

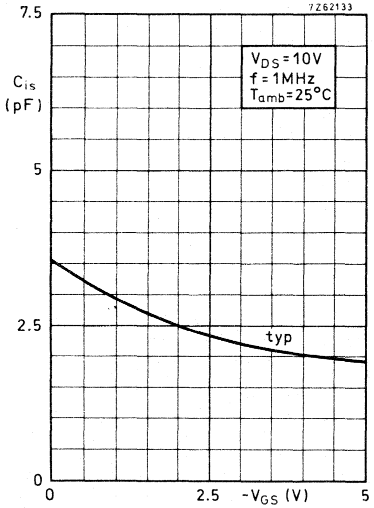


Fig. 13.

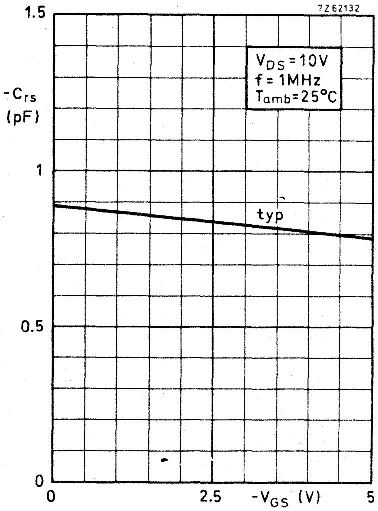


Fig. 14.

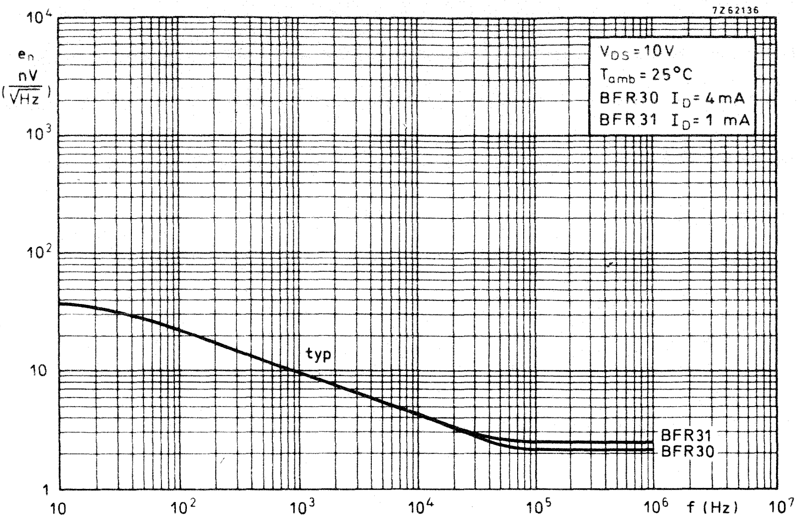

7Z62136
e_n
($\frac{nV}{\sqrt{Hz}}$)
10^4
10^3
10^2
10
1
10
10^2
10^3
10^4
10^5
10^6
f (Hz)
10^7
V_{DS} = 10V
T_{amb} = 25°C
BFR30 I_D = 4 mA
BFR31 I_D = 1 mA
typ
BFR31
BFR30

Fig. 15.

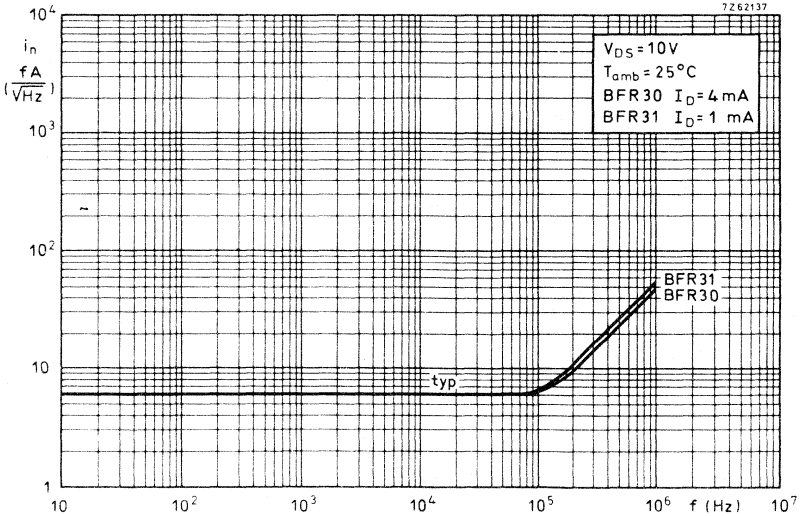

7Z62137
i_n
($\frac{fA}{\sqrt{Hz}}$)
10^4
10^3
10^2
10
1
10
10^2
10^3
10^4
10^5
10^6
f (Hz)
10^7
V_{DS} = 10V
T_{amb} = 25°C
BFR30 I_D = 4 mA
BFR31 I_D = 1 mA
typ
BFR31
BFR30

Fig. 16.

N-CHANNEL JUNCTION FIELD-EFFECT TRANSISTOR

Symmetrical n-channel silicon junction field-effect transistor, designed primarily for use as a source follower with the input protected against successive voltage surges by a forward and reverse integrated diode.

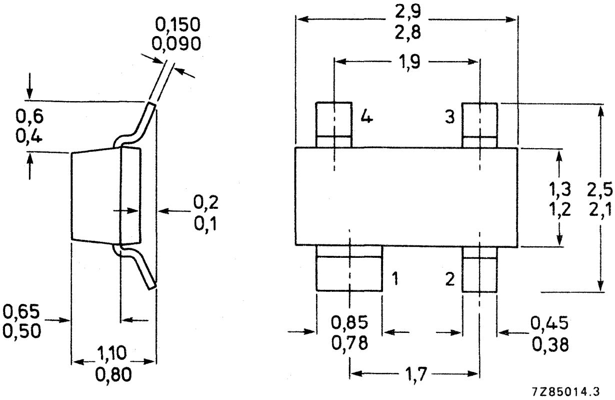
QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Gate-source voltage (open drain)	$-V_{GS}$	max.	30	V
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	max.	200	mW
Drain current				
V_{DS} = 6 V; V_{GS} = 0: BFR101A	I_{DSS}		0,2 to 1,5	mA
V_{DS} = 6 V; V_{GS} = 0: BFR101B	I_{DSS}		1,0 to 5,0	mA
Transfer admittance (common source)				
V_{DS} = 6 V; V_{GS} = 0; f = 1 kHz: BFR101A	$\lvert y_{fs} \rvert$	>	1,2	mS
V_{DS} = 6 V; V_{GS} = 0; f = 1 kHz: BFR101B	$\lvert y_{fs} \rvert$	>	2,5	mS

MECHANICAL DATA

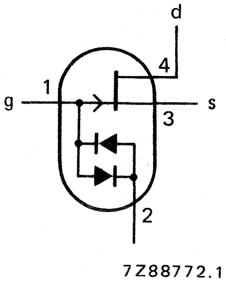
Dimensions in mm

Fig. 1 SOT-143.



Marking code

BFR101A = M97
BFR101B = M98



7Z88772.1

See also *Soldering recommendations.*

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Drain current (d.c.)	I_D	max.	20	mA
Gate current (d.c.)	I_G	max.	10	mA
Total power dissipation up to T_{amb} = 60 °C*	P_{tot}	max.	200	mW
Storage temperature	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air*	$R_{th\ j\text{-}a}$	=	460	K/W

CHARACTERISTICS with source connected to case for all measurements

T_{amb} = 25 °C unless otherwise specified

		BFR101A		BFR101B	
Gate leakage current V_{DS} = 6 V; I_D = 10 μA	$-I_G$	<	5	5	nA
Drain current* V_{DS} = 6 V; V_{GS} = 0	I_{DSS}		0,2 to 1,5	1 to 5	mA
Gate-source cut-off voltage V_{DS} = 6 V; I_D = 1 μA	$-V_{(P)GS}$		0,2 to 1	0,5 to 2,5	V
Small-signal common-source characteristics V_{DS} = 6 V; V_{GS} = 0					
Transfer admittance* f = 1 kHz	$\lvert y_{fs}\rvert$	>	1,2	2,5	mS
→ Output admittance at f = 1 kHz**	$\lvert y_{os}\rvert$	typ.	10	50	mS
Input capacitance at f = 1 MHz diodes not connected	C_{is}	<	5	5	pF
Diode capacitance V_D = 0; source and drain not connected	C_d	typ.	0,7	0,7	pF
Diode forward voltage $\pm I_F$ = 10 mA	V_F		0,7 to 1,2	0,7 to 1,2	V

---

* Device mounted on a ceramic substrate of 8 mm x 10 mm x 0,6 mm.

** Measured under pulse conditions: t_p = 100 ms; $\delta \leqslant 0{,}1$.

MATCHED N-CHANNEL FETS

Matched pair of symmetrical n-channel silicon planar epitaxial junction field-effect transistors in TO-72 metal envelopes, mounted together in a metal S-clip.

These devices are intended for low level differential amplifiers.

QUICK REFERENCE DATA

Characteristics measured at T_{amb} = 25 °C; I_D = 0,5 mA; V_{DG} = 15 V

			BFS21	BFS21A	
Gate cut-off current	I_G	<	0,5	0,5	nA
Gate -source voltage difference	$\|\Delta V_{GS}\|$	<	20	10	mV
Thermal drift of gate-source voltage difference	$\left\|\frac{d\Delta V_{GS}}{dT}\right\|$	<	75	40	µV/K
Difference in transfer impedance	$\left\|\Delta \frac{1}{g_{fs}}\right\|$	<	15	7,5	Ω
Difference in penetration factor	$\left\|\Delta \frac{g_{os}}{g_{fs}}\right\|$	<	1	0,5	mV/V
Common mode rejection ratio	CMRR	>	60	66	dB

MECHANICAL DATA

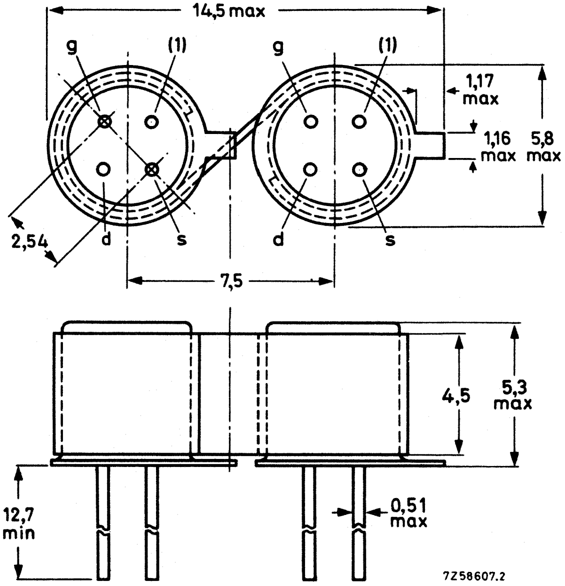
SOT-52

TOTAL DEVICE

Dimensions in mm

MECHANICAL DATA

SOT-52



(1) = shield lead (connected to case).

Maximum lead diameter is guaranteed only for 12,7 mm.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage between any 2 terminals	V	max.	30	V
Drain current	I_D	max.	4	mA
Gate current	I_G	max.	0,5	mA
Total power dissipation up to T_{amb} = 100 °C	P_{tot}	max.	30	mW
Operating ambient temperature	T_{amb}	−20 to + 100		°C

CHARACTERISTICS (total device) T_{amb} = 25 °C unless otherwise specified

		BFS21	BFS21A	
Drain current ratio				
V_{DG} = 15 V; V_{GS} = 0; T_j = 25 °C	$\frac{I_{D1-S1S}}{I_{D2-S2S}}$	$>$ 0.95 $<$ 1.05	0.95 1.05	
Gate-source voltage difference				
I_D = 500 μA; V_{DG} = 15 V	$\lvert \Delta V_{GS} \rvert$	$<$ 20	10	mV
I_D = 100 μA; V_{DG} = 15 V	$\lvert \Delta V_{GS} \rvert$	$<$ 20	10	mV
Thermal drift of gate-source voltage difference				
I_D = 500 μA; V_{DG} = 15 V	$\left\lvert \frac{d\ \Delta V_{GS}}{dT} \right\rvert$	$<$ 75	40	μV/°C
I_D = 100 μA; V_{DG} = 15 V	$\left\lvert \frac{d\ \Delta V_{GS}}{dT} \right\rvert$	$<$ 75	40	μV/°C
Change of gate-source voltage difference with ambient temperature				
T_{amb} = 25 to 100 °C				
I_D = 500 μA; V_{DG} = 15 V	$\lvert \Delta V_{GS}(T_{amb2}) - \Delta V_{GS}(T_{amb1}) \rvert$	$<$ 6	3	mV
I_D = 100 μA; V_{DG} = 15 V	$\lvert \Delta V_{GS}(T_{amb2}) - \Delta V_{GS}(T_{amb1}) \rvert$	$<$ 6	3	mV
Difference of penetration factors [1]				
I_D = 500 μA; V_{DG} = 15 V	$\left\lvert \Delta \frac{g_{os}}{g_{fs}} \right\rvert$	$<$ 1	0.5	10^{-3}
I_D = 100 μA; V_{DG} = 15 V	$\left\lvert \Delta \frac{g_{os}}{g_{fs}} \right\rvert$	$<$ 1	0.5	10^{-3}
Difference of transfer impedances [2]				
I_D = 500 μA; V_{DG} = 15 V	$\left\lvert \Delta \frac{1}{g_{fs}} \right\rvert$	$<$ 15	7.5	Ω
I_D = 100 μA; V_{DG} = 15 V	$\left\lvert \Delta \frac{1}{g_{fs}} \right\rvert$	$<$ 75	37.5	Ω

---

[1] The difference between the penetration factors is equal to the ratio of the change of the gate-source voltage difference to the change of drain-gate voltage, at constant drain current.

$$\left(\Delta \frac{g_{os}}{g_{fs}} = \frac{d\ \Delta V_{GS}}{d\ V_{DG}} \text{ at } I_D = \text{constant}\right)$$

[2] The difference between the transfer impedances is equal to the ratio of the change of the gate-source voltage difference to the change of drain current, at constant drain-gate voltage.

$$\left(\Delta \frac{1}{g_{fs}} = \frac{d\ \Delta V_{GS}}{d\ I_D} \text{ at } V_{DG} = \text{constant}\right)$$

CHARACTERISTICS (continued) (total device)

Common mode rejection ratio [1]			BFS21	BFS21A	
I_D = 500 μA; V_{DG} = 15 V	CMRR	>	60	66	dB
I_D = 100 μA; V_{DG} = 15 V	CMRR	>	60	66	dB

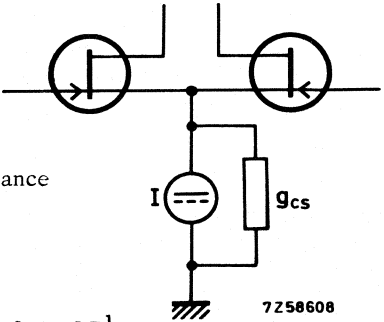
INDIVIDUAL TRANSISTOR

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages				
Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Currents				
Drain current	I_D	max.	20	mA
Gate current	I_G	max.	10	mA
Power dissipation				
Total power dissipation up to $T_{amb} = 25^{o}$	P_{tot}	max.	300	mW
Temperatures				
Storage temperature	T_{stg}		-65 to +200	°C
Junction temperature	T_j	max.	200	°C

THERMAL RESISTANCE

From junction to ambient in free air
(for individual transistor without S-clip) $R_{th\ j-a}$ = 0.59 °C/m



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[1] Common mode rejection ratio

$$(\mathrm{CMRR})^{-1} = \Delta \frac{g_{os}}{g_{fs}} + \tfrac{1}{2}\, g_{cs}\, \Delta \frac{1}{g_{fs}}$$

where g_{cs} in this formula is the output conductance of the summing current source.

The guaranteed values of CMRR apply at $g_{cs} = 0.1\ \mu\Omega^{-1}$

CHARACTERISTICS (individual transistor) $T_{amb} = 25\,^{o}C$ unless otherwise specified

Gate cut-off current				
$I_D = 500\ \mu A$; $V_{DS} = 15\ V$	I_G	$<$	0.5	nA
$I_D = 500\ \mu A$; $V_{DS} = 15\ V$; $T_{amb} = 100\ ^{o}C$	I_G	$<$	25	nA
Drain current				
$V_{DS} = 15\ V$, $V_{GS} = 0$, $T_j = 25\ ^{o}C$	I_{DSS}	$>$	1	mA
Gate-source cut-off voltage				
$I_D = 0.5\ nA$, $V_{DS} = 15\ V$	$-V_{(P)GS}$	$<$	6	V
Transfer conductance at f = 1 kHz				
$I_D = 500\ \mu A$; $V_{DS} = 15\ V$	g_{fs}	$>$	1.0	$m\Omega^{-1}$
Output conductance at f = 1 kHz				
$I_D = 500\ \mu A$; $V_{DS} = 15\ V$	g_{os}	$<$	15	$\mu\Omega^{-1}$
Input capacitance at f = 1 MHz				
$I_D = 500\ \mu A$; $V_{DS} = 15\ V$	C_{is}	$<$	5	pF
Feedback capacitance at f = 1 MHz				
$I_D = 500\ \mu A$; $V_{DS} = 15\ V$	C_{rs}	$<$	0.75	pF
Equivalent noise voltage				
f = 10 Hz				
$I_D = 500\ \mu A$; $V_{DS} = 15\ V$	$V_n/\sqrt{B}$	$<$	200	$nV/\sqrt{Hz}$
$V_{DS} = 15\ V$, $V_{GS} = 0$	$V_n/\sqrt{B}$	$<$	75	$nV/\sqrt{Hz}$

N-CHANNEL SILICON FET

N-channel silicon epitaxial planar junction field-effect transistor in a microminiature plastic envelope. The transistor is intended for low level general purpose amplifiers in thick and thin-film circuits.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	25	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25	V
Total power dissipation up to $T_{amb} = 65\ ^{o}C$	P_{tot}	max.	250	mW
Drain current $V_{DS} = 10\ V;\ V_{GS} = 0$	I_{DSS}	$>$ $<$	0,2 1,5	mA mA
Transfer admittance (common source) $I_D = 0,2\ mA;\ V_{DS} = 10\ V;\ f = 1\ kHz$	$\lvert y_{fs} \rvert$	$>$	0,5	mA/V
Equivalent noise voltage $V_{DS} = 10\ V;\ I_D = 200\ \mu A;\ B = 0,6$ to $100\ Hz$	V_n	$<$	0,5	μV

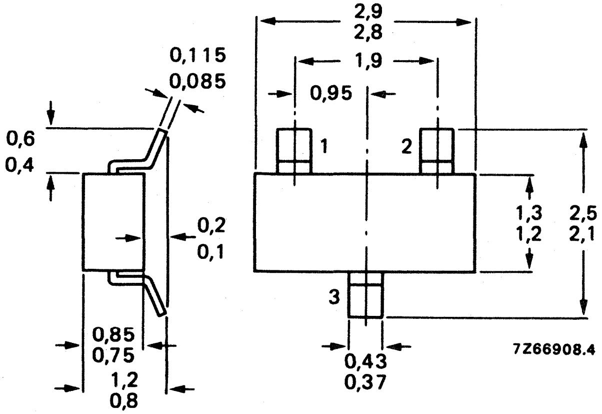
MECHANICAL DATA

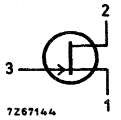
Dimensions in mm

Marking code

BFT46 = M3

Fig. 1 SOT-23.





See also *Soldering recommendations.*

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	25	V
Drain-gate voltage (open source)	V_{DGO}	max.	25	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25	V
Drain current	I_D	max.	10	mA
Gate current	I_G	max.	5	mA
Total power dissipation up to T_{amb} = 65 °C**	P_{tot}	max.	250	mW
Storage temperature	T_{stg}		−65 to +175	°C
Junction temperature	T_j	max.	175	°C

THERMAL CHARACTERISTICS*

$$R_{th\ j\text{-}t} + R_{th\ t\text{-}s} + R_{th\ s\text{-}a} = \frac{T_j - T_{amb}}{P}$$

Thermal resistance

From junction to tab	$R_{th\ j\text{-}t}$	=	60	K/W
From tab to soldering points	$R_{th\ t\text{-}s}$	=	280	K/W
From soldering points to ambient**	$R_{th\ s\text{-}a}$	=	90	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off current $-V_{GS}$ = 10 V; V_{DS} = 0	$-I_{GSS}$	<	0,2	nA
Drain current ** V_{DS} = 10 V; V_{GS} = 0	I_{DSS}	> <	0,2 1,5	mA mA
Gate-source voltage I_D = 50 μA; V_{DS} = 10 V	$-V_{GS}$	> <	0,1 1,0	V V
Gate-source cut-off voltage I_D = 0,5 nA; V_{DS} = 10 V	$-V_{(P)GS}$	<	1,2	V
Y parameters at f = 1 kHz; V_{DS} = 10 V; V_{GS} = 0; T_{amb} = 25 °C				
Transfer admittance	$\lvert y_{fs}\rvert$	>	1,0	mA/V
Output admittance	$\lvert y_{os}\rvert$	<	10	μA/V
V_{DS} = 10 V; I_D = 200 μA;				
Transfer admittance	$\lvert y_{fs}\rvert$	>	0,5	mA/V
Output admittance	$\lvert y_{os}\rvert$	<	5	μA/V

---

* See *Thermal characteristics* in chapter GENERAL.

** Mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

Input capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0; T_{amb} = 25 °C	C_{is}	$<$	5 pF
Feedback capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0; T_{amb} = 25 °C	C_{rs}	$<$	1,5 pF
Equivalent noise voltage V_{DS} = 10 V; I_D = 200 μA; T_{amb} = 25 °C B = 0,6 to 100 Hz	V_n	$<$	0,5 μV

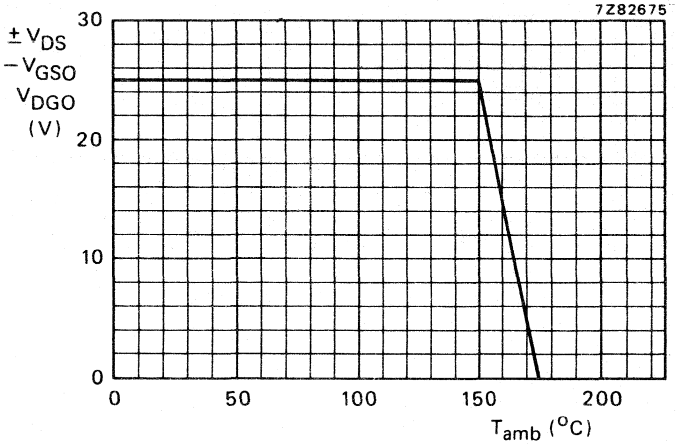


Fig. 2 Voltage derating curve.

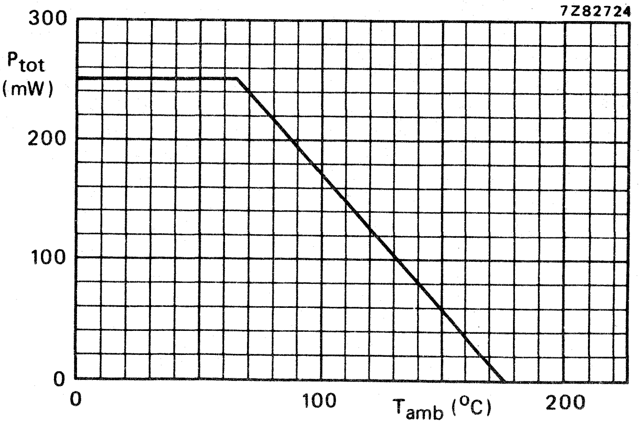


Fig. 3 Power derating curve.

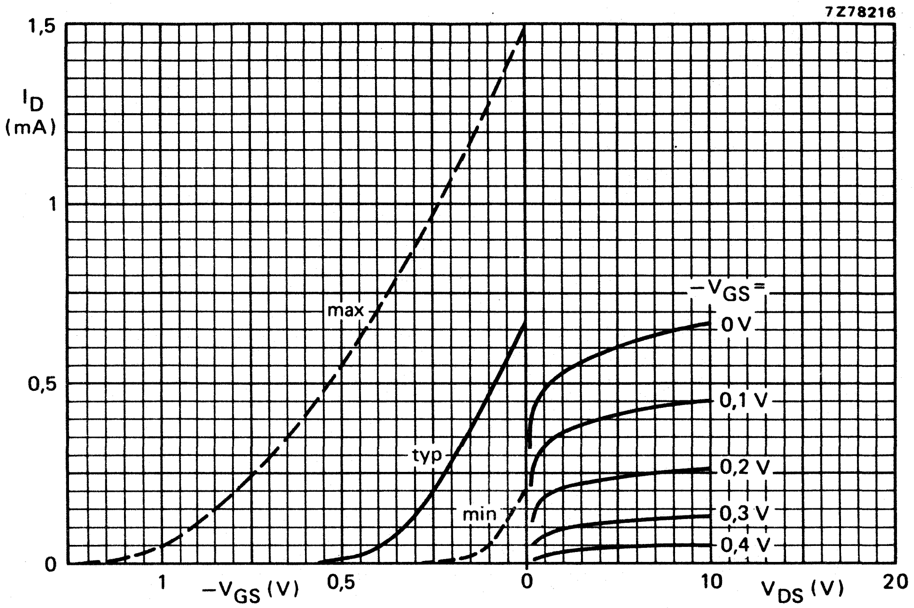


Fig. 4 Typical values. V_{DS} = 10 V; T_j = 25 °C.

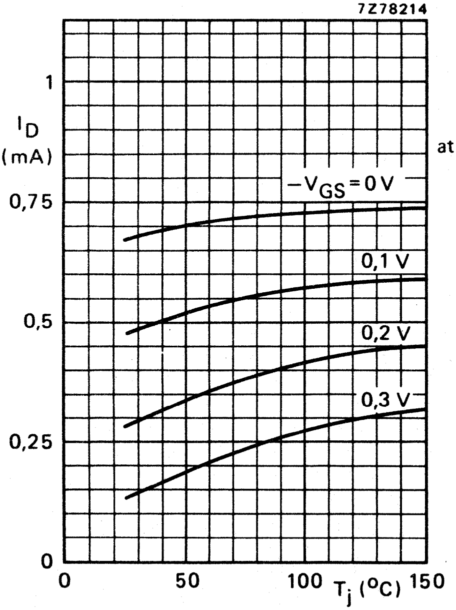


Fig. 5 Typical values. V_{DS} = 10 V.

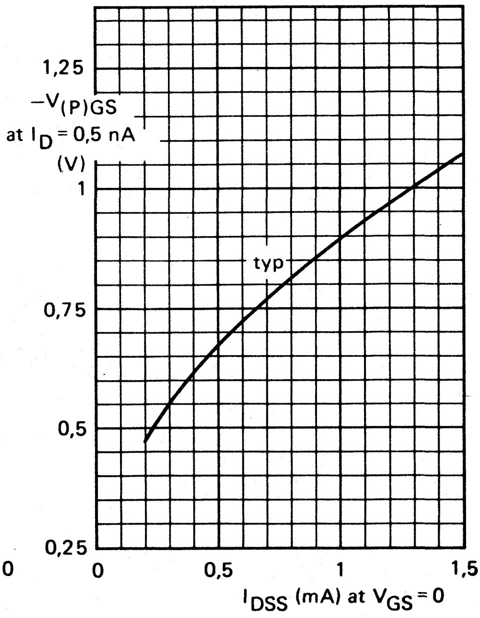


Fig. 6 Correlation between $-V_{(P)GS}$ and I_{DSS}. V_{DS} = 10 V; T_j = 25 °C.

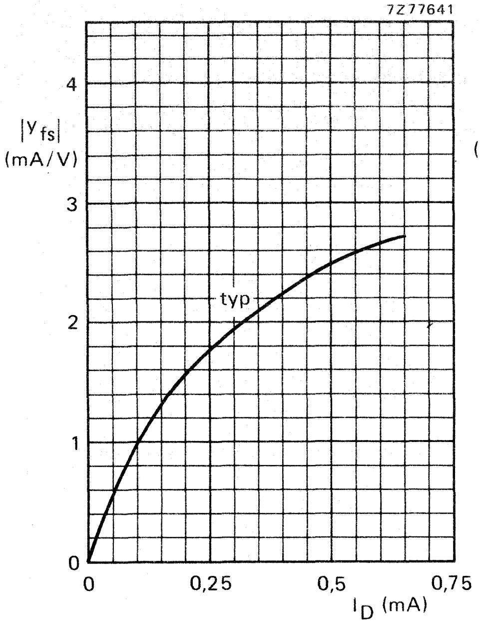


Fig. 7.

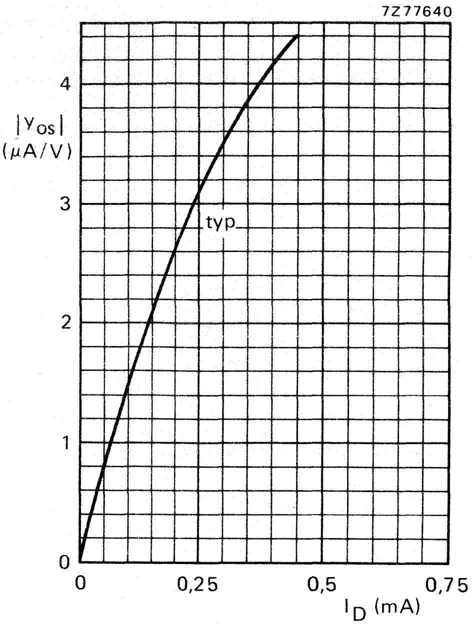


Fig. 8.

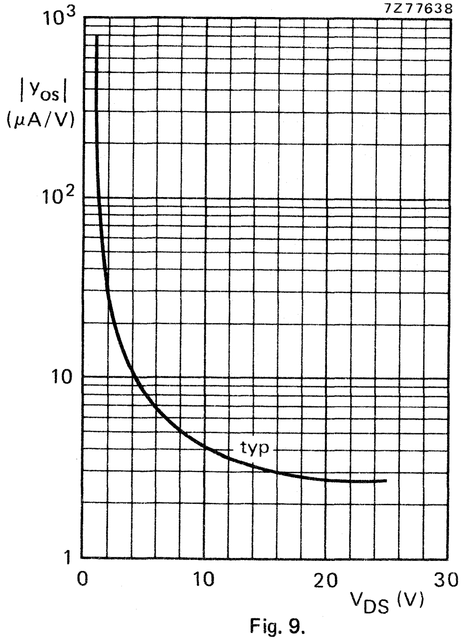


Fig. 9.

Fig. 7 $|y_{fs}|$ versus I_D.
$V_{DS} = 10$ V; f = 1 kHz; $T_{amb} = 25$ °C.

Fig. 8 $|y_{os}|$ versus I_D.
$V_{DS} = 10$ V; f = 1 kHz; $T_{amb} = 25$ °C.

Fig. 9 $|y_{os}|$ versus V_{DS}.
$I_D = 0{,}4$ mA; f = 1 kHz; $T_{amb} = 25$ °C.

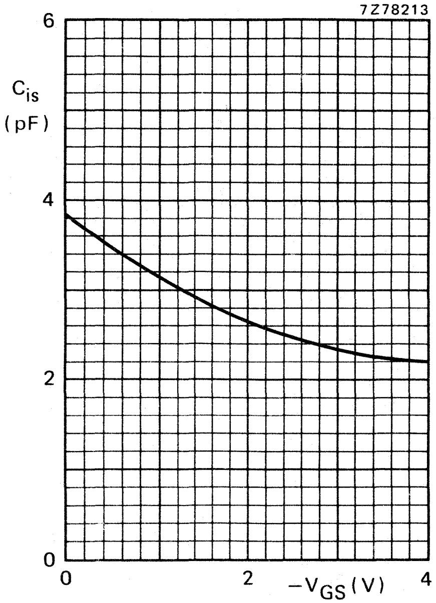


Fig. 10.

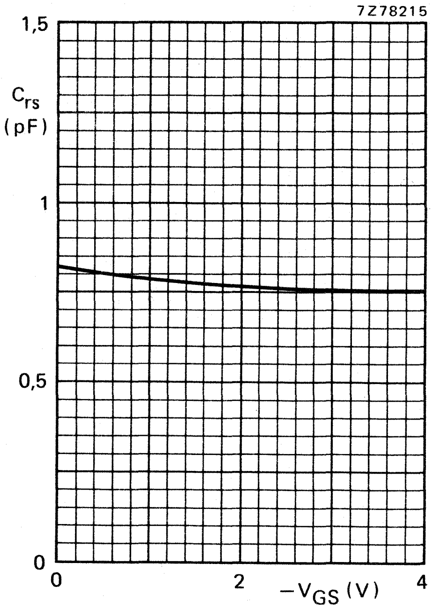


Fig. 11.

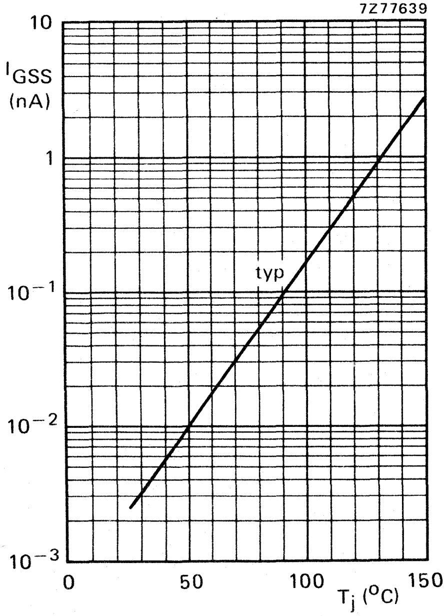


Fig. 12.

Fig.10 Typical values.
V_{DS} = 10 V, T_{amb} = 25 °C.

Fig.11 Typical values.
V_{DS} = 10 V, T_{amb} = 25 °C.

Fig.12 I_{GSS} versus T_j.
$-V_{GSS}$ = 10V; V_{DS} = 0.

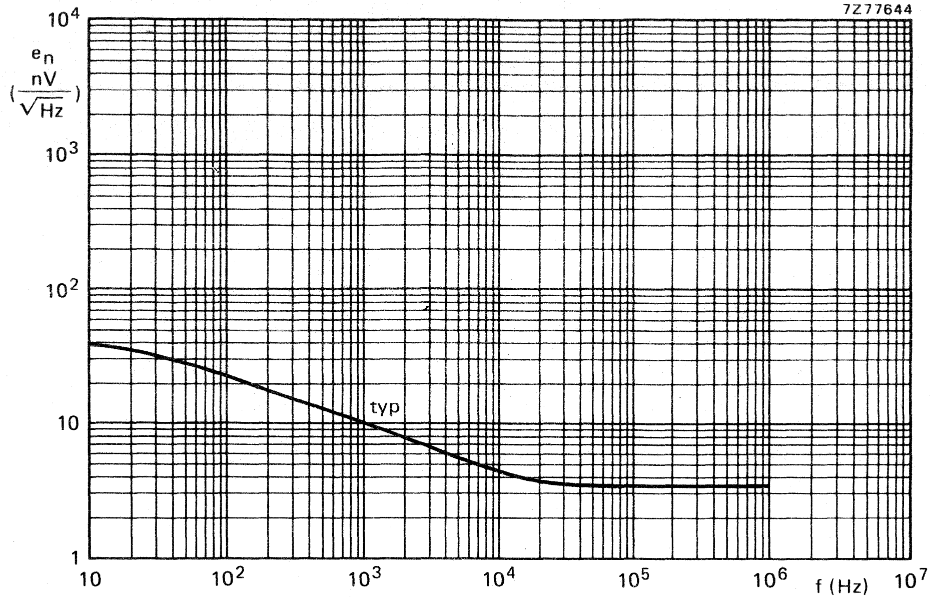


Fig. 13 $V_{DS} = 10$ V; $I_D = 0{,}2$ mA; $T_{amb} = 25$ °C.

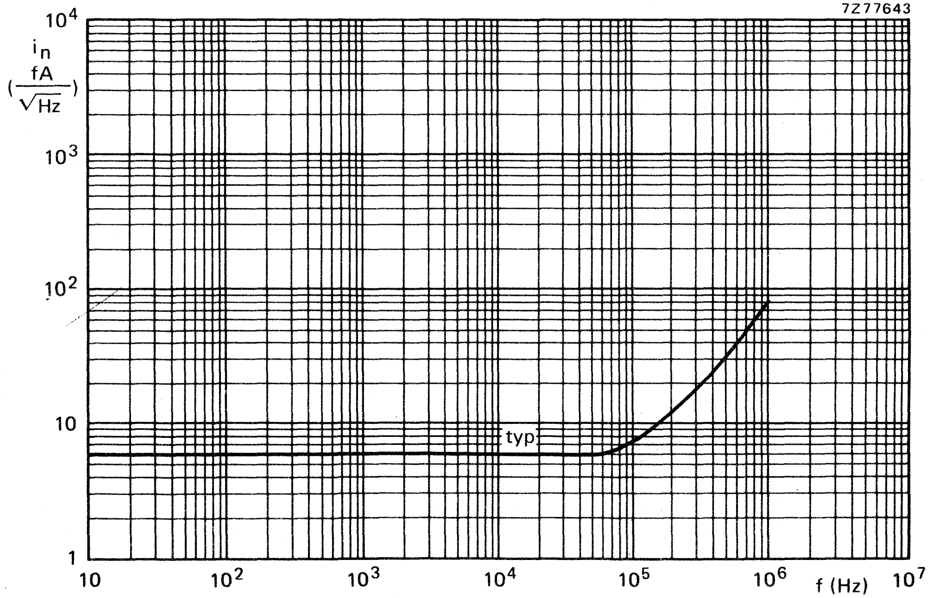


Fig. 14 $V_{DS} = 10$ V; $I_D = 0{,}2$ mA; $T_{amb} = 25$ °C.

N-CHANNEL SILICON FETS

Symmetrical n-channel silicon planar epitaxial junction field-effect transistors in TO-72 metal envelopes with the shield lead connected to the case. The transistors are designed for broad band amplifiers (0 to 300 MHz). Their very low noise at low frequencies makes these devices very suitable for differential amplifiers, electro-medical and nuclear detector preamplifiers.

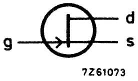
QUICK REFERENCE DATA

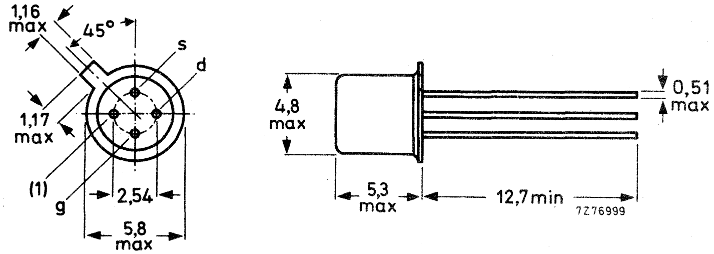
Drain-source voltage	$\pm V_{DS}$	max.	30		V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30		V
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300		mW
			BFW10	**BFW11**	
Drain current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	$>$ $<$	8 20	4 10	mA mA
Gate-source cut-off voltage I_D = 0,5 nA; V_{DS} = 15 V	$-V_{(P)GS}$	$<$	8	6	V
Feedback capacitance at f = 1 MHz V_{DS} = 15 V; V_{GS} = 0	C_{rs}	$<$	0,80	0,80	pF
Transfer admittance (common source) V_{DS} = 15 V; V_{GS} = 0; f = 200 MHz	$\lvert y_{fs} \rvert$	$>$	3,2	3,2	mA/V
Noise figure at V_{DS} = 15 V; V_{GS} = 0 f = 100 MHz; R_G = 1 kΩ	F	$<$	2,5	2,5	dB
Equivalent noise voltage f = 10 Hz	$V_n/\sqrt{B}$	$<$	75	75	$nV/\sqrt{Hz}$

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-72.





(1) = shield lead connected to case

Accessories: 56246 (distance disc).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages				
Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Currents				
Drain current	I_D	max.	20	mA
Gate current	I_G	max.	10	mA
Power dissipation				
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300	mW
Temperatures				
Storage temperature	T_{stg}		−65 to +200	°C
Junction temperature	T_j	max.	200	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	0.59	°C/mW

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

			BFW10	BFW11	
Gate cut-off current					
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	<	0.1	0.1	nA
$-V_{GS}$ = 20 V; V_{DS} = 0; T_j = 150 °C	$-I_{GSS}$	<	0.5	0.5	μA
Drain current [1]					
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	8	4	mA
		<	20	10	mA
Gate-source voltage					
I_D = 400 μA; V_{DS} = 15 V	$-V_{GS}$	>	2.0		V
		<	7.5		V
I_D = 50 μA; V_{DS} = 15 V	$-V_{GS}$	>		1.25	V
		<		4.0	V
Gate-source cut-off voltage					
I_D = 0.5 nA; V_{DS} = 15 V	$-V_{(P)GS}$	<	8	6	V
y parameters					
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C f = 1 kHz Transfer admittance	$\lvert y_{fs} \rvert$	>	3.5	3.0	mA/V
		<	6.5	6.5	mA/V
Output admittance	$\lvert y_{os} \rvert$	<	85	50	μA/V
f = 1 MHz Input capacitance	C_{is}	typ.	4	4	pF
		<	5	5	pF
Feedback capacitance	C_{rs}	typ.	0.6	0.6	pF
		<	0.80	0.80	pF
f = 200 MHz Transfer admittance	$\lvert y_{fs} \rvert$	>	3.2	3.2	mA/V
Input conductance	g_{is}	<	800	800	μA/V
Output conductance	g_{os}	<	200	100	μA/V
Noise figure at f = 100 MHz; R_G = 1 kΩ					
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C input tuned to minimum noise	F	<	2.5	2.5	dB
Equivalent noise voltage					
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C f = 10 Hz	$V_n/\sqrt{B}$	<	75	75	nV/$\sqrt{\text{Hz}}$

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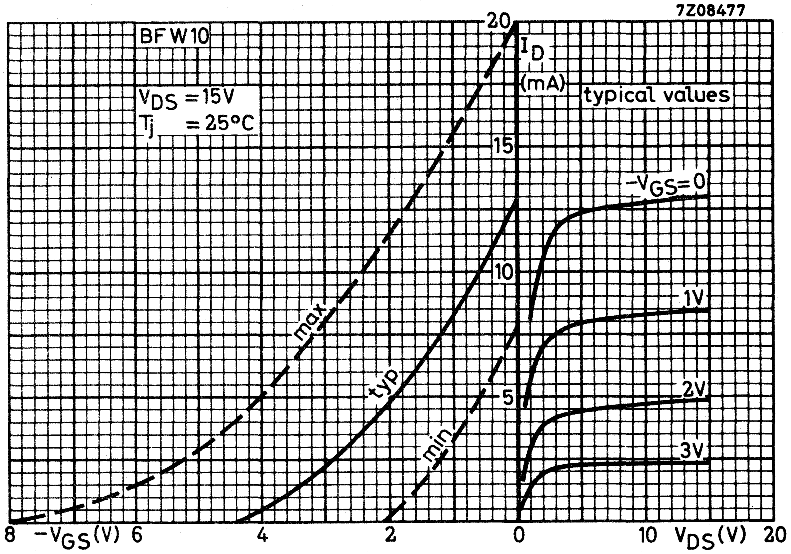
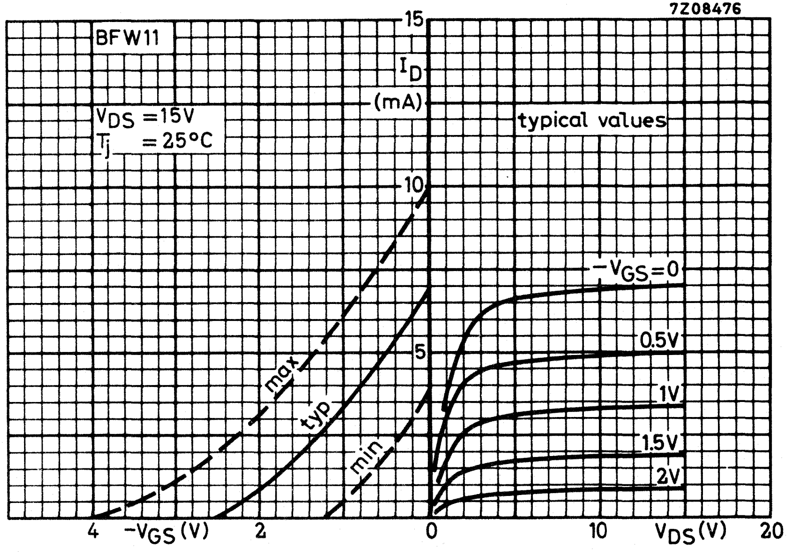
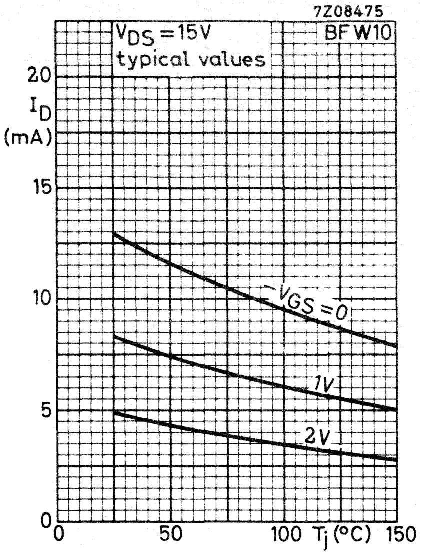
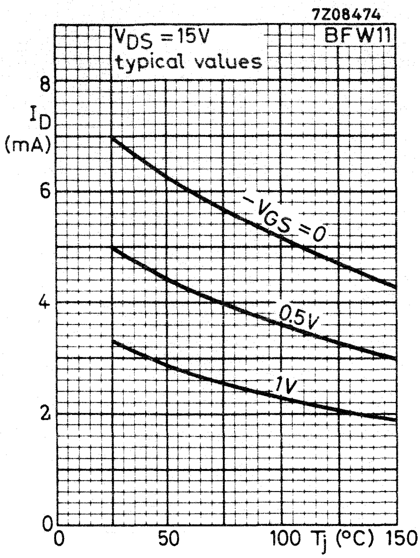
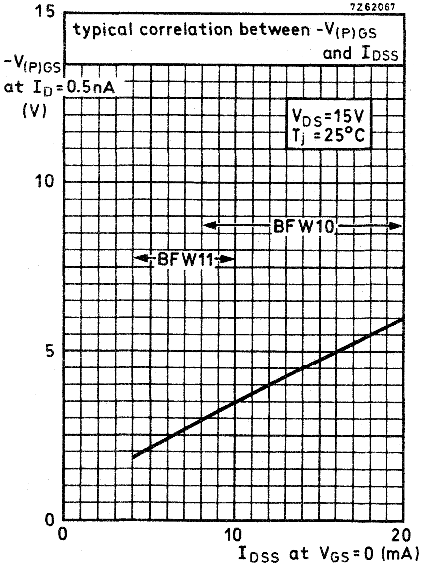
[1] Measured under pulse conditions.

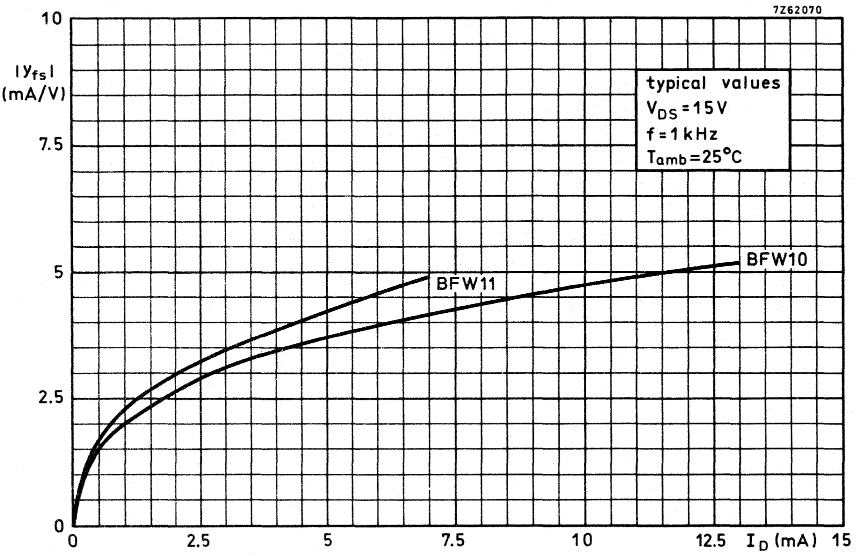

7Z08477
BF W10
V_{DS} = 15V
T_j = 25°C
I_D (mA)
20
15
10
5
typical values
$-V_{GS}$=0
1V
2V
3V
max
typ
min
8
$-V_{GS}$(V)
6
4
2
0
10
V_{DS}(V)
20

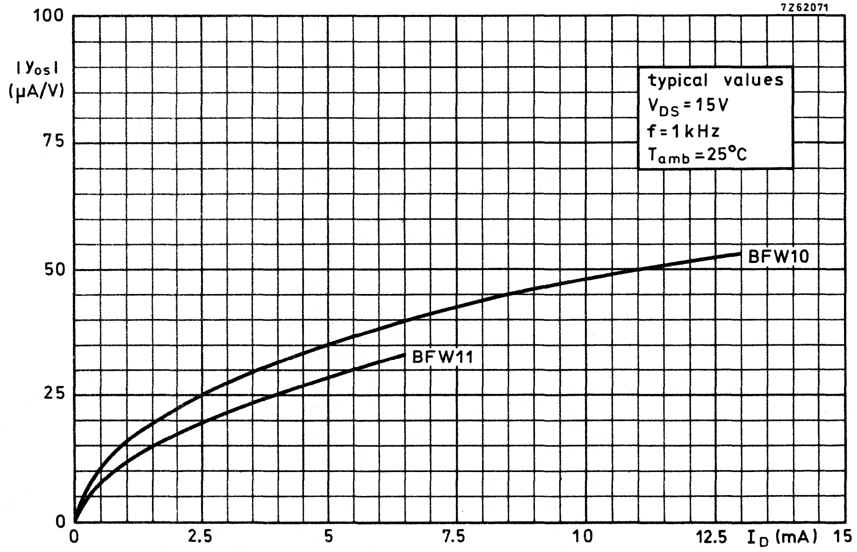

7Z08476
BFW11
V_{DS} = 15V
T_j = 25°C
I_D (mA)
15
10
5
typical values
$-V_{GS}$=0
0.5V
1V
1.5V
2V
max
typ
min
4
$-V_{GS}$(V)
2
0
10
V_{DS}(V)
20

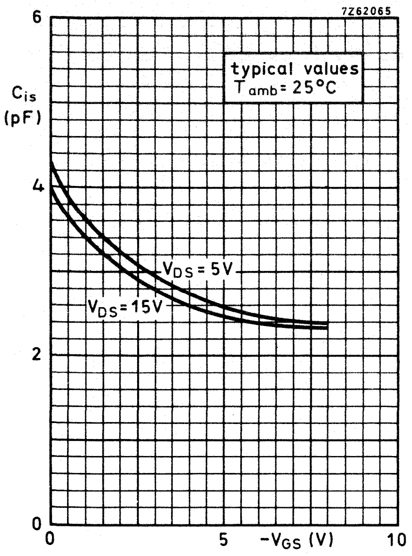

7Z08475
V_{DS} = 15V
typical values
BFW10
I_D (mA)
0
5
10
15
20
$-V_{GS}$ = 0
1V
2V
0
50
100
150
T_j (°C)

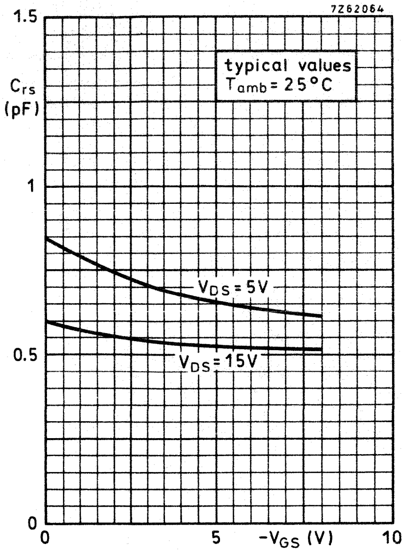

7Z08474
V_{DS} = 15V
typical values
BFW11
I_D (mA)
0
2
4
6
8
$-V_{GS}$ = 0
0.5V
1V
0
50
100
150
T_j (°C)

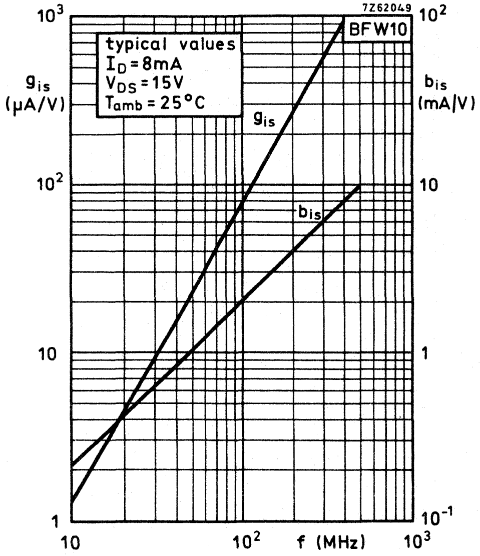

7Z62067
typical correlation between $-V_{(P)GS}$ and I_{DSS}
$-V_{(P)GS}$ at I_D = 0.5nA (V)
0
5
10
15
V_{DS} = 15V
T_j = 25°C
BFW10
BFW11
0
10
20
I_{DSS} at V_{GS} = 0 (mA)

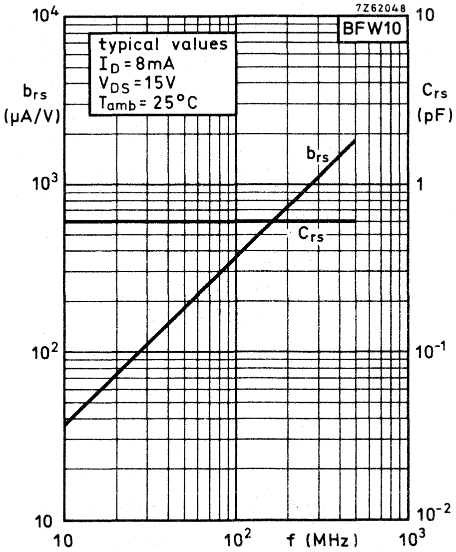

7Z62070
10
$|y_{fs}|$ (mA/V)
7.5
5
2.5
0
0
2.5
5
7.5
10
12.5
I_D (mA)
15
typical values
V_{DS} = 15 V
f = 1 kHz
T_{amb} = 25°C
BFW10
BFW11

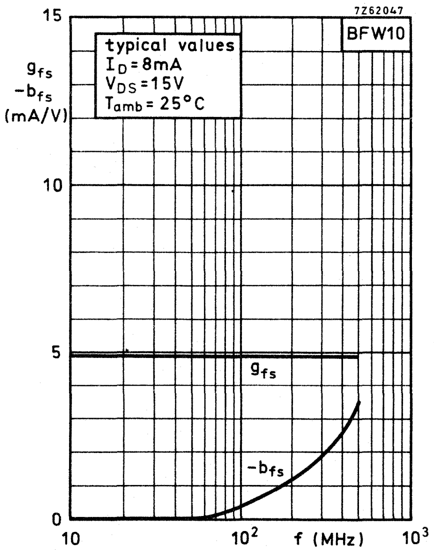

7Z62071
100
$|y_{os}|$ (μA/V)
75
50
25
0
0
2.5
5
7.5
10
12.5
I_D (mA)
15
typical values
V_{DS} = 15 V
f = 1 kHz
T_{amb} = 25°C
BFW10
BFW11

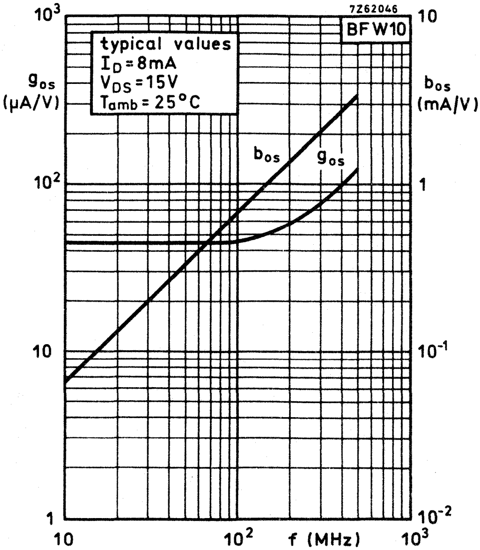

7Z62065
typical values
T_{amb} = 25°C
C_{is} (pF)
6
4
2
0
V_{DS} = 5V
V_{DS} = 15V
0
5
$-V_{GS}$ (V)
10

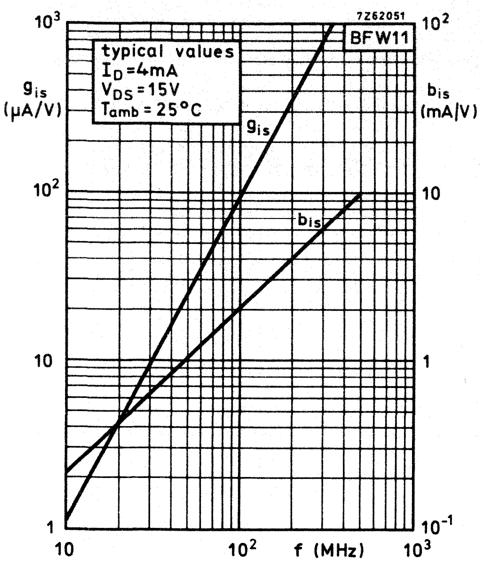

7Z62064
typical values
T_{amb} = 25°C
C_{rs} (pF)
1.5
1
0.5
0
V_{DS} = 5V
V_{DS} = 15V
0
5
$-V_{GS}$ (V)
10

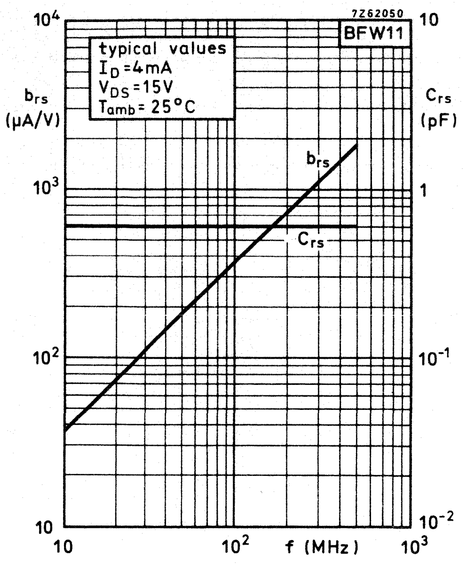

7Z62049
BFW10
typical values
I_D = 8mA
V_{DS} = 15V
T_{amb} = 25°C
g_{is} (μA/V)
b_{is} (mA/V)
g_{is}
b_{is}
10^3
10^2
10
1
10^2
10
1
10^{-1}
10
10^2
f (MHz)
10^3

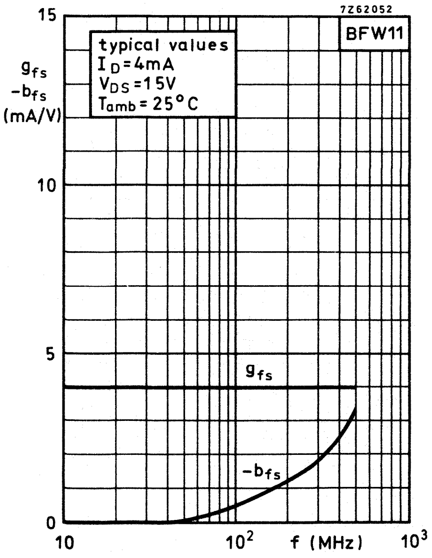

7Z62048
BFW10
typical values
I_D = 8mA
V_{DS} = 15V
T_{amb} = 25°C
b_{rs} (μA/V)
C_{rs} (pF)
b_{rs}
C_{rs}
10^4
10^3
10^2
10
10
1
10^{-1}
10^{-2}
10
10^2
f (MHz)
10^3

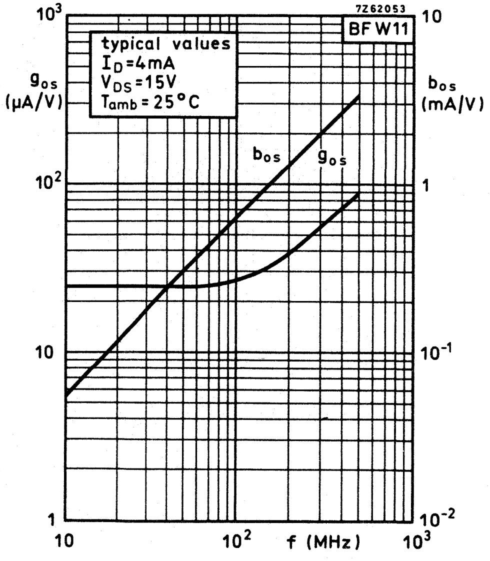

7Z62047
BFW10
typical values
I_D = 8mA
V_{DS} = 15V
T_{amb} = 25°C
g_{fs} $-b_{fs}$ (mA/V)
g_{fs}
$-b_{fs}$
15
10
5
0
10
10^2
f (MHz)
10^3

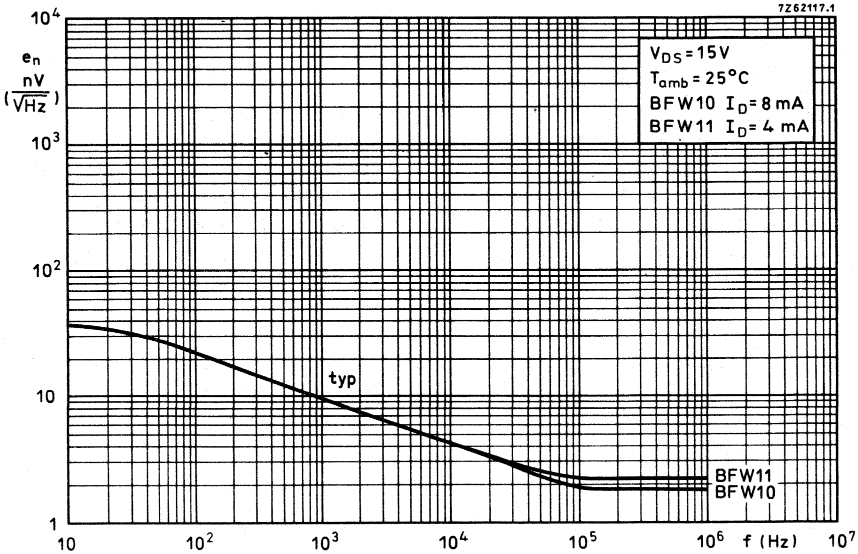

7Z62046
BFW10
typical values
I_D = 8mA
V_{DS} = 15V
T_{amb} = 25°C
g_{os} (μA/V)
b_{os} (mA/V)
b_{os}
g_{os}
10^3
10^2
10
1
10
1
10^{-1}
10^{-2}
10
10^2
f (MHz)
10^3

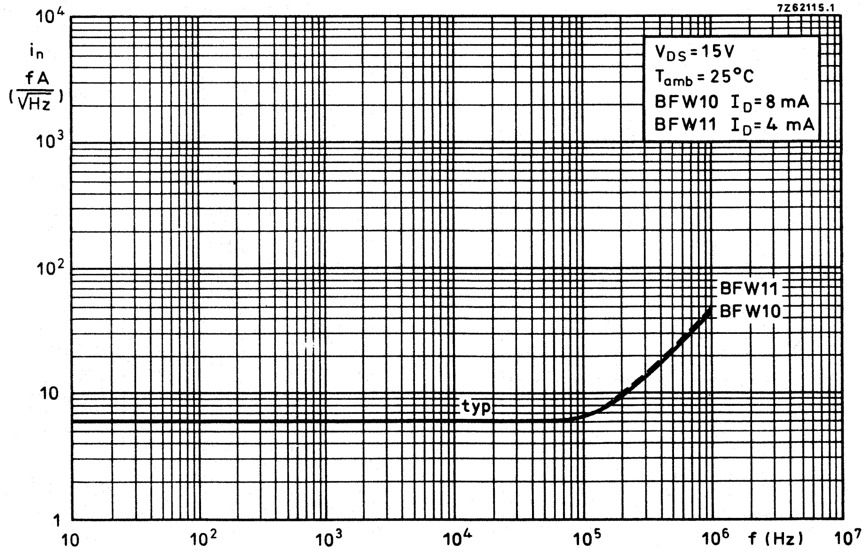

7Z62051
BFW11
typical values
I_D = 4mA
V_{DS} = 15V
T_{amb} = 25°C
g_{is} (μA/V)
b_{is} (mA/V)
g_{is}
b_{is}
10^3
10^2
10
1
10^2
10
1
10^{-1}
10
10^2
f (MHz)
10^3

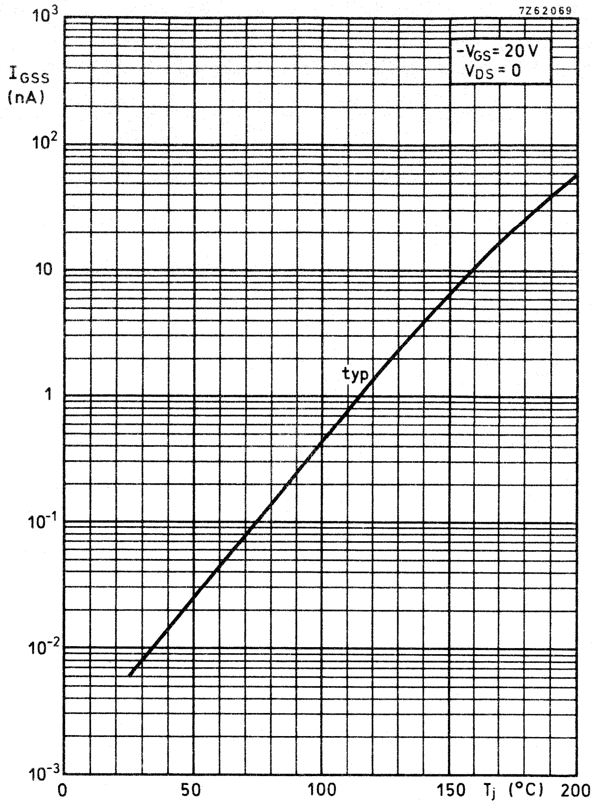

7Z62050
BFW11
typical values
I_D = 4mA
V_{DS} = 15V
T_{amb} = 25°C
b_{rs} (μA/V)
C_{rs} (pF)
b_{rs}
C_{rs}
10^4
10^3
10^2
10
10
1
10^{-1}
10^{-2}
10
10^2
f (MHz)
10^3


7Z62052
BFW11
typical values
I_D = 4mA
V_{DS} = 15V
T_{amb} = 25°C
g_{fs} $-b_{fs}$ (mA/V)
g_{fs}
$-b_{fs}$
15
10
5
0
10
10^2
f (MHz)
10^3


7Z62053
BFW11
typical values
I_D = 4mA
V_{DS} = 15V
T_{amb} = 25°C
g_{os} (μA/V)
b_{os} (mA/V)
b_{os}
g_{os}
10^3
10^2
10
1
10
1
10^{-1}
10^{-2}
10
10^2
f (MHz)
10^3


7Z62117.1
e_n
nV/√Hz
10^4
10^3
10^2
10
1
V_{DS} = 15V
T_{amb} = 25°C
BFW10 I_D = 8 mA
BFW11 I_D = 4 mA
typ
BFW11
BFW10
10
10^2
10^3
10^4
10^5
10^6
f (Hz)
10^7


7Z62115.1
i_n
fA/√Hz
10^4
10^3
10^2
10
1
V_{DS} = 15V
T_{amb} = 25°C
BFW10 I_D = 8 mA
BFW11 I_D = 4 mA
typ
BFW11
BFW10
10
10^2
10^3
10^4
10^5
10^6
f (Hz)
10^7


7Z62069
$-V_{GS} = 20$ V
$V_{DS} = 0$
I_{GSS}
(nA)
10^3
10^2
10
1
10^{-1}
10^{-2}
10^{-3}
typ
0
50
100
150
T_j (°C)
200

N-CHANNEL SILICON FETS

Symmetrical n-channel silicon planar epitaxial junction field-effect transistors in TO-72 metal envelopes with the shield lead connected to the case. The transistors are intended for battery powered equipment and other low current-low voltage applications.

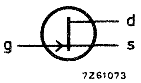
QUICK REFERENCE DATA

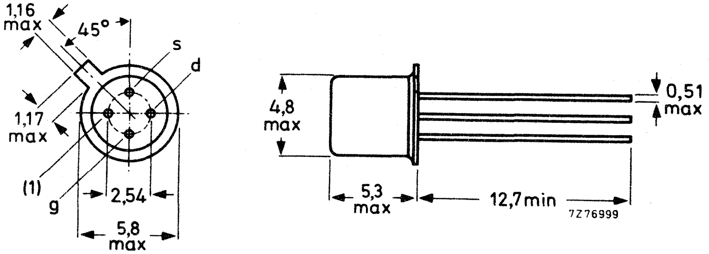
			BFW12	BFW13	
Drain-source voltage	$\pm V_{DS}$	max.	30		V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30		V
Total power dissipation up to T_{amb} = 110 °C	P_{tot}	max.	150		mW
Drain current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	1	0,2	mA
		<	5	1,5	mA
Gate-source cut-off voltage I_D = 0,5 nA; V_{DS} = 15 V	$-V_{(P)GS}$	<	2,5	1,2	V
Feedback capacitance at f = 1 MHz V_{DS} = 15 V; V_{GS} = 0	C_{rs}	<	0,80	0,80	pF
Transfer admittance (common source) V_{DS} = 15 V; I_D = 200 μA; f = 1 kHz	$\lvert y_{fs} \rvert$	>	0,5	0,5	mA/V
Equivalent noise voltage V_{DS} = 15 V; I_D = 200 μA B = 0,6 to 100 Hz	V_n	<	0,5	0,5	μV

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-72.





(1) = shield lead connected to case

Accessories: 56246 (distance disc).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V

Currents

Drain current	I_D	max.	10	mA
Gate current	I_G	max.	5	mA

Power dissipation

Total power dissipation up to T_{amb} = 110 °C	P_{tot}	max.	150	mW

Temperatures

Storage temperature	T_{stg}	−65 to	+200	°C
Junction temperature	T_j	max.	200	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	0.59	°C/mW

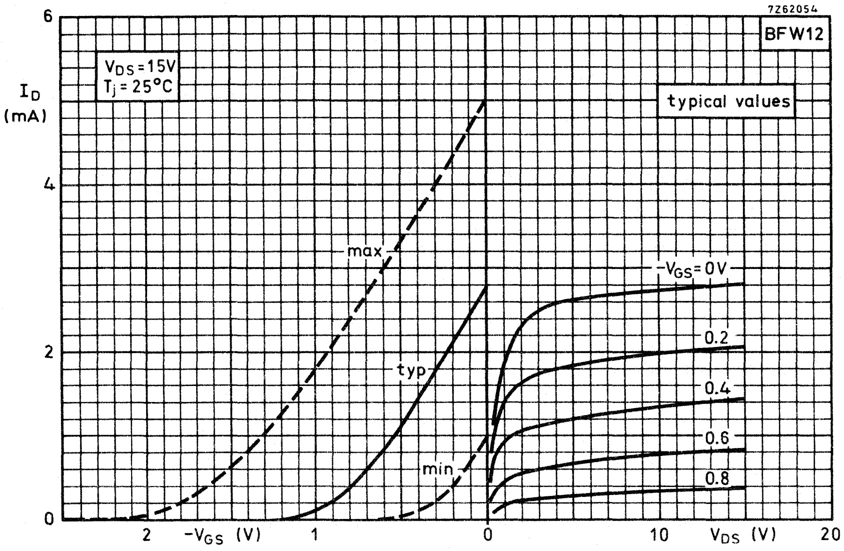
CHARACTERISTICS

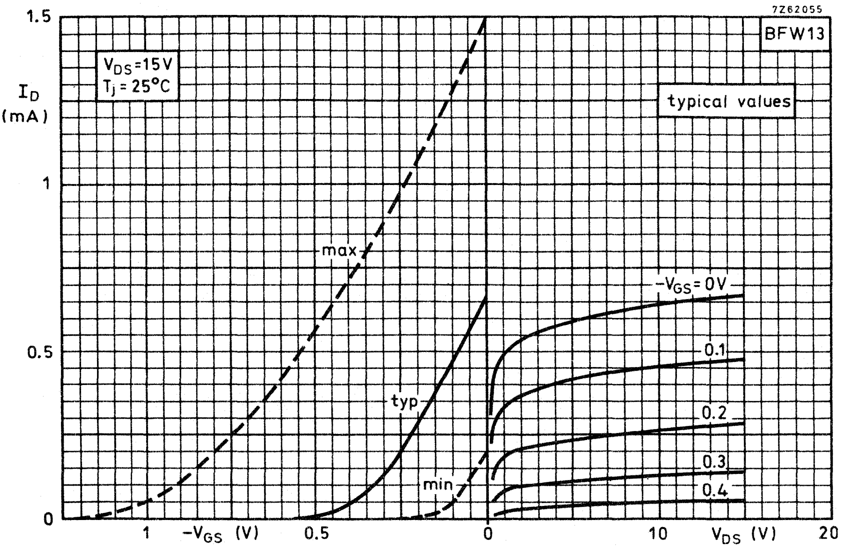
T_j = 25 °C unless otherwise specified

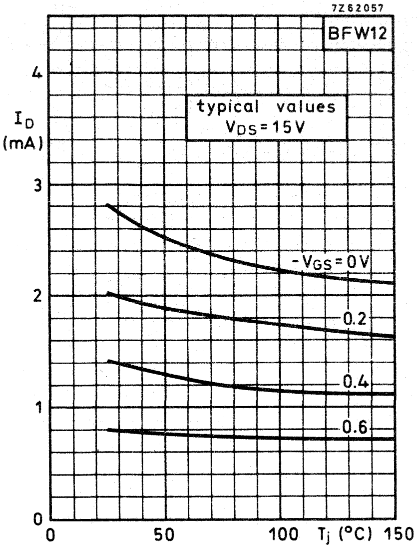
			BFW12	BFW13	
Gate cut-off current					
$-V_{GS}$ = 10 V; V_{DS} = 0	$-I_{GSS}$	<	0.1	0.1	nA
$-V_{GS}$ = 10 V; V_{DS} = 0; T_j = 150 °C	$-I_{GSS}$	<	0.1	0.1	µA
Drain current [1]					
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	1	0.2	mA
		<	5	1.5	mA
Gate-source voltage					
I_D = 50 µA; V_{DS} = 15 V	$-V_{GS}$	>	0.5	0.1	V
		<	2.0	1.0	V
Gate-source cut-off voltage					
I_D = 0.5 nA; V_{DS} = 15 V	$-V_{(P)GS}$	<	2.5	1.2	V
y parameters at f = 1 kHz; T_{amb} = 25 °C					
V_{DS} = 15 V; V_{GS} = 0					
Transfer admittance	$\|y_{fs}\|$	>	2.0	1.0	mA/V
Output admittance	$\|y_{os}\|$	<	30	10	µA/V
V_{DS} = 15 V; I_D = 500 µA					
Transfer admittance	$\|y_{fs}\|$	>	1.5	-	mA/V
Output admittance	$\|y_{os}\|$	<	10	-	µA/V
V_{DS} = 15 V; I_D = 200 µA					
Transfer admittance	$\|y_{fs}\|$	>	0.5	0.5	mA/V
Output admittance	$\|y_{os}\|$	<	5	5	µA/V
f = 1 MHz; T_{amb} = 25 °C					
V_{DS} = 15 V; V_{GS} = 0					
Input capacitance	C_{iss}	<	5	5	pF
Feedback capacitance	C_{rs}	<	0.80	0.80	pF
Equivalent noise voltage					
V_{DS} = 15 V; I_D = 200 µA; T_{amb} = 25 °C B = 0.6 to 100 Hz	V_n	<	0.5	0.5	µV

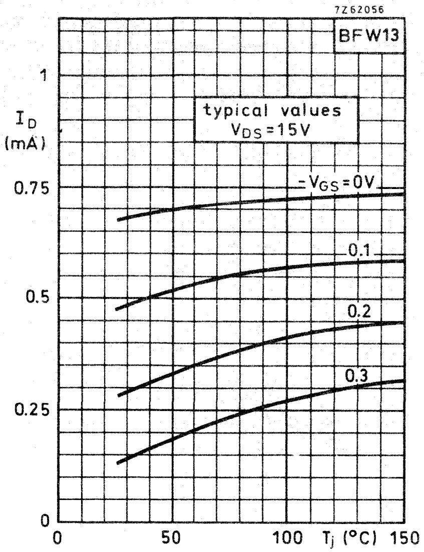
---

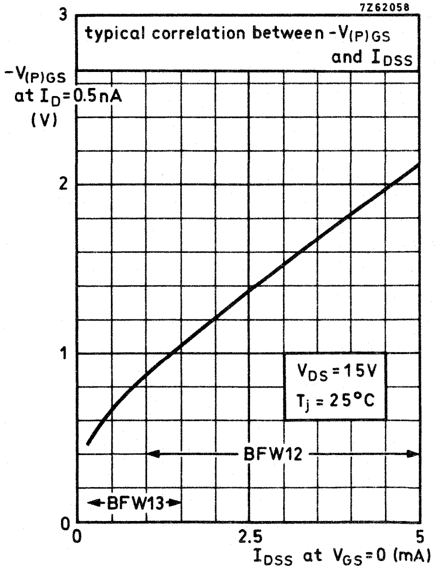
[1] Measured under pulse conditions.

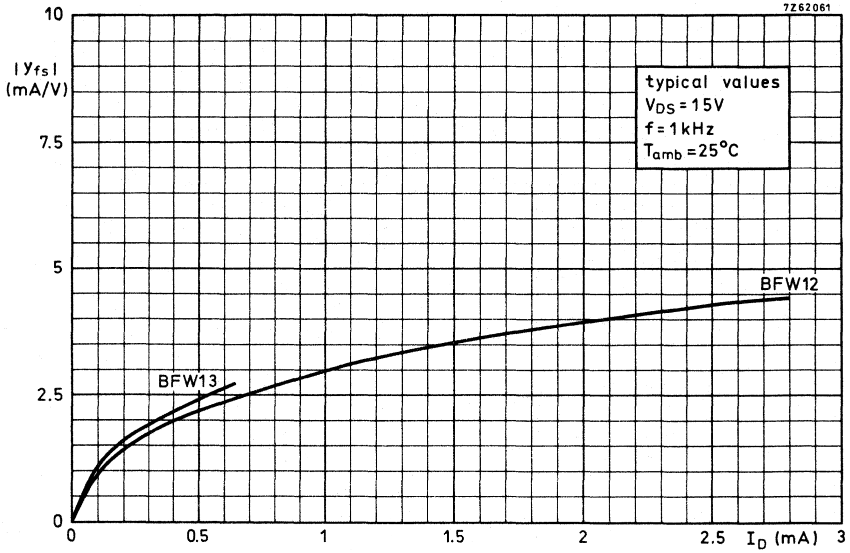

7Z62054
BFW12
V_{DS} = 15 V
T_j = 25 °C
I_D (mA)
typical values
6
4
2
0
max
typ
min
$-V_{GS}$ = 0 V
0.2
0.4
0.6
0.8
2
$-V_{GS}$ (V)
1
0
10
V_{DS} (V)
20

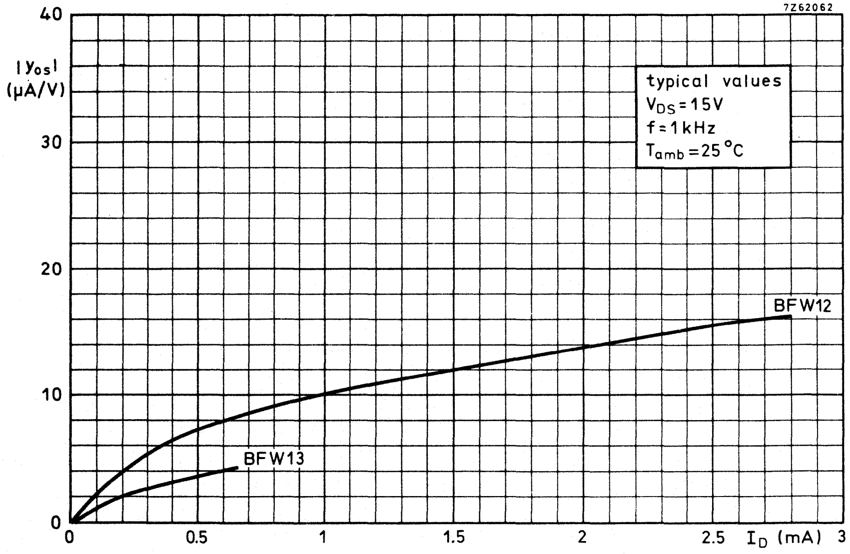

7Z62055
BFW13
V_{DS} = 15 V
T_j = 25 °C
I_D (mA)
typical values
1.5
1
0.5
0
max
typ
min
$-V_{GS}$ = 0 V
0.1
0.2
0.3
0.4
1
$-V_{GS}$ (V)
0.5
0
10
V_{DS} (V)
20

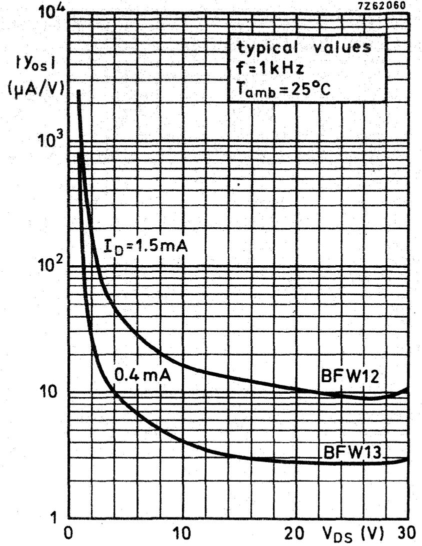

7Z62057
BFW12
typical values
$V_{DS} = 15\,V$
I_D (mA)
4
3
2
1
0
$-V_{GS} = 0\,V$
0.2
0.4
0.6
0
50
100
T_j (°C)
150

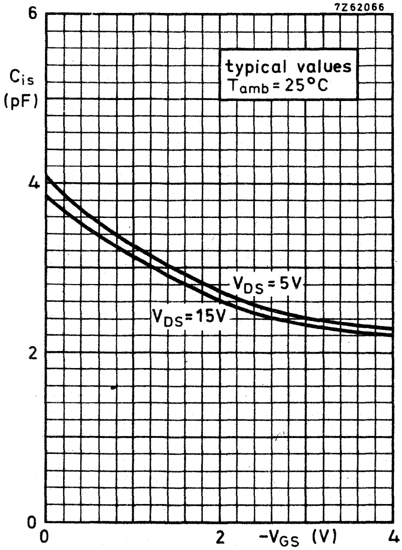

7Z62056
BFW13
typical values
$V_{DS} = 15\,V$
I_D (mA)
1
0.75
0.5
0.25
0
$-V_{GS} = 0\,V$
0.1
0.2
0.3
0
50
100
T_j (°C)
150

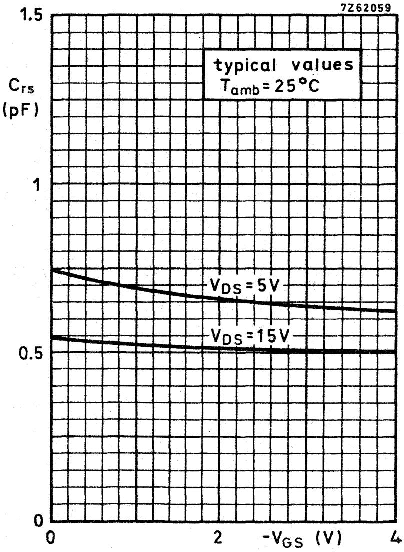

7Z62058
typical correlation between $-V_{(P)GS}$ and I_{DSS}
$-V_{(P)GS}$ at $I_D = 0.5\,nA$ (V)
3
2
1
0
$V_{DS} = 15\,V$
$T_j = 25\,°C$
BFW12
BFW13
0
2.5
5
I_{DSS} at $V_{GS} = 0$ (mA)

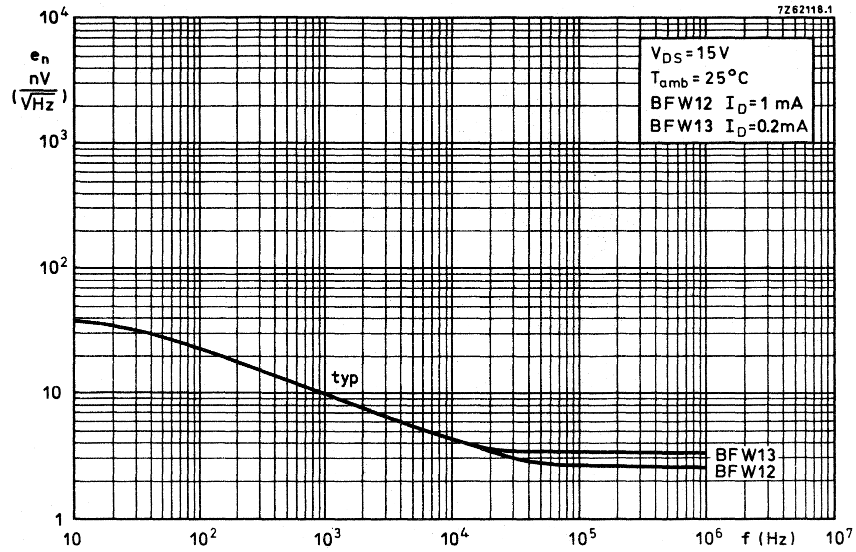

7Z62061
|y_fs| (mA/V)
10
7.5
5
2.5
0
typical values
V_DS = 15V
f = 1kHz
T_amb = 25°C
BFW12
BFW13
0
0.5
1
1.5
2
2.5
I_D (mA)
3

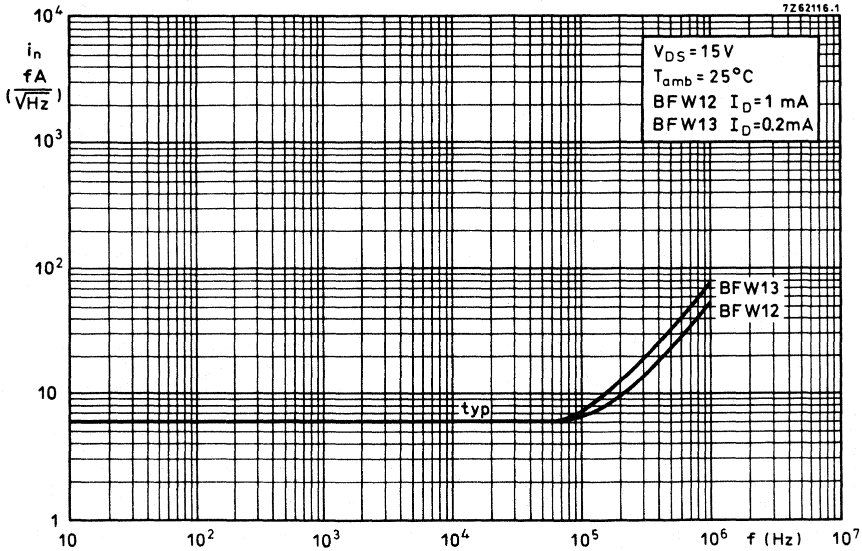

7Z62062
|y_os| (µA/V)
40
30
20
10
0
typical values
V_DS = 15V
f = 1kHz
T_amb = 25°C
BFW12
BFW13
0
0.5
1
1.5
2
2.5
I_D (mA)
3

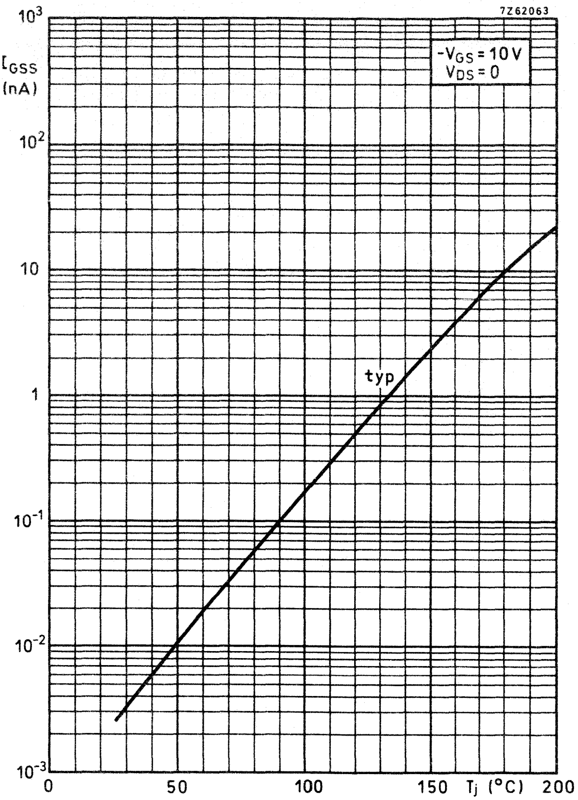

7Z62060
$|y_{os}|$ (μA/V)
10^4
10^3
10^2
10
1
typical values
f = 1 kHz
T_{amb} = 25°C
I_D = 1.5 mA
0.4 mA
BFW12
BFW13
0
10
20
V_{DS} (V)
30


7Z62066
C_{is} (pF)
6
4
2
0
typical values
T_{amb} = 25°C
V_{DS} = 5V
V_{DS} = 15V
0
2
$-V_{GS}$ (V)
4


7Z62059
C_{rs} (pF)
1.5
1
0.5
0
typical values
T_{amb} = 25°C
V_{DS} = 5V
V_{DS} = 15V
0
2
$-V_{GS}$ (V)
4


7Z62118.1
e_n
nV
$(\sqrt{Hz})$
10^4
10^3
10^2
10
1
10
10^2
10^3
10^4
10^5
10^6
f (Hz)
10^7
$V_{DS} = 15 V$
$T_{amb} = 25 °C$
BFW12 $I_D = 1$ mA
BFW13 $I_D = 0.2$ mA
typ
BFW13
BFW12


7Z62116.1
i_n
fA
$(\sqrt{Hz})$
10^4
10^3
10^2
10
1
10
10^2
10^3
10^4
10^5
10^6
f (Hz)
10^7
$V_{DS} = 15 V$
$T_{amb} = 25 °C$
BFW12 $I_D = 1$ mA
BFW13 $I_D = 0.2$ mA
typ
BFW13
BFW12


7Z62063
I_{GSS} (nA)
10^3
10^2
10
1
10^{-1}
10^{-2}
10^{-3}
$-V_{GS} = 10\,V$
$V_{DS} = 0$
typ
0
50
100
150
T_j (°C)
200

N-CHANNEL SILICON FET

Symmetrical n-channel silicon planar epitaxial junction field-effect transistor in a TO-72 metal envelope with the shield lead connected to the case. The transistor is designed for general purpose amplifiers.

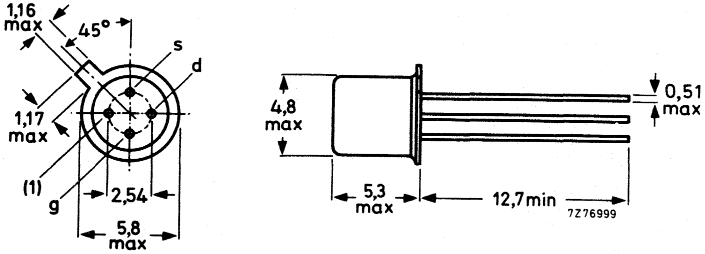
QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	25	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25	V
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300	mW
Drain current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}		2 to 20	mA
Gate-source cut-off voltage I_D = 1,0 nA; V_{DS} = 15 V	$-V_{(P)GS}$	$<$	8	V
Feedback capacitance at f = 1 MHz V_{DS} = 15 V; V_{GS} = 0	C_{rs}	$<$	2,0	pF
Transfer admittance (common source) V_{DS} = 15 V; V_{GS} = 0; f = 10 MHz	$\lvert y_{fs} \rvert$	$>$	1,6	mA/V

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-72.



(1) = shield lead connected to case

Accessories: 56246 (distance disc).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	25	V
Drain-gate voltage (open source)	V_{DGO}	max.	25	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25	V
Drain current	I_D	max.	20	mA
Gate current	I_G	max.	10	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300	mW
Storage temperature	T_{stg}		−65 to + 200	°C
Junction temperature	T_j	max.	200	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\,j\text{-}a}$	=	590	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents				
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	$<$	1,0	nA
$-V_{GS}$ = 20 V; V_{DS} = 0; T_j = 150 °C	$-I_{GSS}$	$<$	1,0	μA
Drain current*				
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}		2 to 20	mA
Gate-source voltage				
I_D = 200 μA; V_{DS} = 15 V	$-V_{GS}$		0,5 to 7,5	V
Gate-source cut-off voltage				
I_D = 1,0 nA; V_{DS} = 15 V	$-V_{(P)GS}$	$<$	8	V
y-parameters (common source)				
V_{DS} = 15 V; V_{GS} = 0				
Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$		2,0 to 6,5	mA/V
at f = 10 MHz		$>$	1,6	mA/V
Output admittance at f = 1 kHz	$\lvert y_{os} \rvert$	$<$	85	μA/V
Input capacitance at f = 1 MHz	C_{is}	$<$	6	pF
Feedback capacitance at f = 1 MHz	C_{rs}	$<$	2,0	pF

---

* Measured under pulse conditions.

N-CHANNEL FETS

Silicon n-channel depletion type junction field-effect transistors in a plastic microminiature envelope intended for application in thick and thin-film circuits. The transistors are intended for low-power, chopper or switching applications in industrial service.

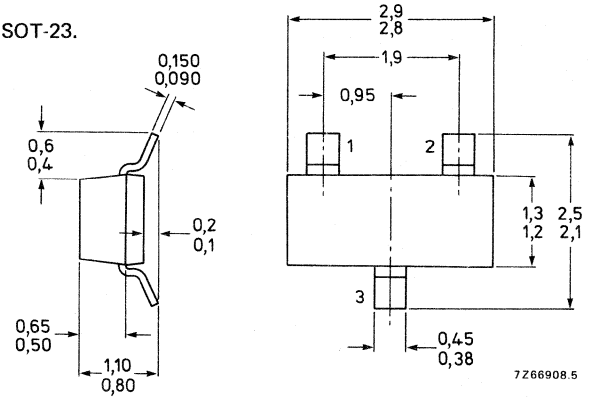
QUICK REFERENCE DATA

			BSR56	BSR57	BSR58	
Drain-source voltage	$\pm V_{DS}$	max.	40	40	40	V
Total power dissipation up to T_{amb} = 65 °C	P_{tot}	max.	250	250	250	mW
Drain current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	$>$	50	20	8	mA
		$<$	–	100	80	mA
Gate-source cut-off voltage V_{DS} = 15 V; I_D = 0,5 nA	$-V_{(P)GS}$	$>$	4	2	0,8	V
		$<$	10	6	4	V
Drain-source resistance (on) at f = 1 kHz I_D = 0; V_{GS} = 0	$r_{ds\ on}$	$<$	25	40	60	Ω
Feedback capacitance at f = 1 MHz $-V_{GS}$ = 10 V; V_{DS} = 0	C_{rs}	$<$	5	5	5	pF
Turn-off time V_{DD} = 10 V; V_{GS} = 0						
I_D = 20 mA; $-V_{GSM}$ = 10 V	t_{off}	$<$	25	–	–	ns
I_D = 10 mA; $-V_{GSM}$ = 6 V	t_{off}	$<$	–	50	–	ns
I_D = 5 mA; $-V_{GSM}$ = 4 V	t_{off}	$<$	–	–	100	ns

MECHANICAL DATA

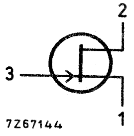
Dimensions in mm

Fig. 1 SOT-23.



Marking code

BSR56 = M4
BSR57 = M5
BSR58 = M6



See also *Soldering Recommendations.*

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage (See Fig. 4)	$\pm V_{DS}$	max.	40	V
Drain-gate voltage (See Fig. 4)	V_{DGO}	max.	40	V
Gate-source voltage (See Fig. 4)	$-V_{GSO}$	max.	40	V
Forward gate current	I_{GF}	max.	50	mA
Total power dissipation up to T_{amb} = 65 °C	P_{tot}	max.	250	mW
Storage temperature	T_{stg}		−55 to + 175	°C
Junction temperature	T_j	max.	175	°C

THERMAL CHARACTERISTICS*

$T_j = P\,(R_{th\,j\text{-}t} + R_{th\,t\text{-}s} + R_{th\,s\text{-}a}) + T_{amb}$

Thermal resistance

From junction to tab	$R_{th\,j\text{-}t}$	=	60	K/W
From tab to soldering points	$R_{th\,t\text{-}s}$	=	280	K/W
From soldering points to ambient**	$R_{th\,s\text{-}a}$	=	90	K/W

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

Gate-source cut-off current $V_{DS} = 0$ V; $-V_{GS} = 20$ V	$-I_{GSS}$	<	1	nA
Drain cut-off current $V_{DS} = 15$ V; $-V_{GS} = 10$ V	I_{DSX}	<	1	nA

			BSR56	BSR57	BSR58	
Drain current ▲ $V_{DS} = 15$ V; $V_{GS} = 0$	I_{DSS}	>	50	20	8	mA
		<	–	100	80	mA
Gate-source breakdown voltage $-I_G = 1\ \mu$A; $V_{DS} = 0$	$-V_{(BR)GSS}$	>	40	40	40	V
Gate-source cut-off voltage $I_D = 0{,}5$ nA; $V_{DS} = 15$ V	$-V_{(P)GS}$	>	4	2	0,8	V
		<	10	6	4	V
Drain-source voltage (on) $I_D = 20$ mA; $V_{GS} = 0$	V_{DSon}	<	750	–	–	mV
$I_D = 10$ mA; $V_{GS} = 0$	V_{DSon}	<	–	500	–	mV
$I_D = 5$ mA; $V_{GS} = 0$	V_{DSon}	<	–	–	400	mV
Drain-source resistance (on) at f = 1 kHz $I_D = 0$; $V_{GS} = 0$	$r_{ds\,on}$	<	25	40	60	Ω

---

* See *Thermal characteristics* in chapter GENERAL.

** Mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

▲ Measured under pulsed conditions; $t_p = 100$ ms; $\delta \leqslant 0{,}1$.

Switching times*
V_{DD} = 10 V; V_{GS} = 0

			BSR56	BSR57	BSR58	
Conditions I_D and $-V_{GSM}$	I_D	=	20	10	5	mA
	$-V_{GSM}$	=	10	6	4	V
Delay time	t_d	<	6	6	10	ns
Rise time	t_r	<	3	4	10	ns
Turn-off time	t_{off}	<	25	50	100	ns

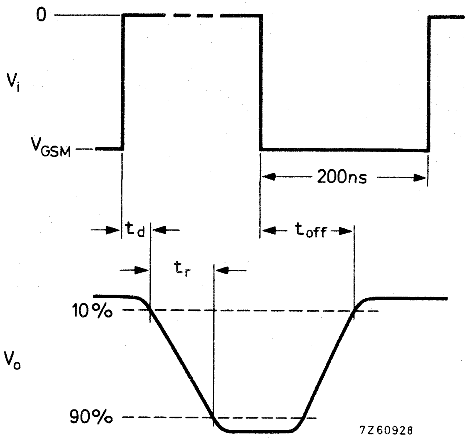


Fig. 2 Switching times waveforms.

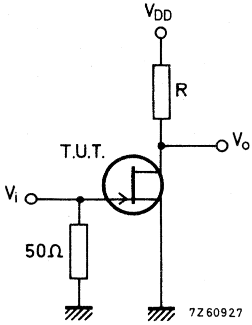


Fig. 3 Test circuit.

BSR56; R = 464 Ω
BSR57; R = 953 Ω
BSR58; R = 1910 Ω

Pulse generator

$t_r = t_f \leqslant 1$ ns
δ = 0,02
Z_o = 50 Ω

Oscilloscope

$t_r \leqslant 0,75$ ns
$R_i \geqslant$ 1 MΩ
$C_i \leqslant$ 2,5 pF

---

* Switching times measured on devices in SOT-18 envelope.

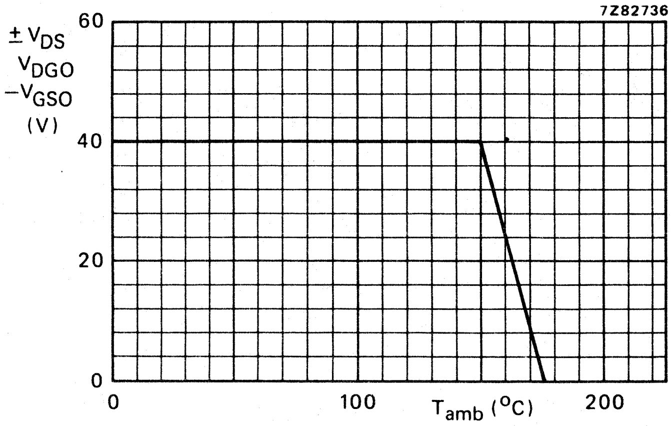


Fig. 4 Voltage derating curve.

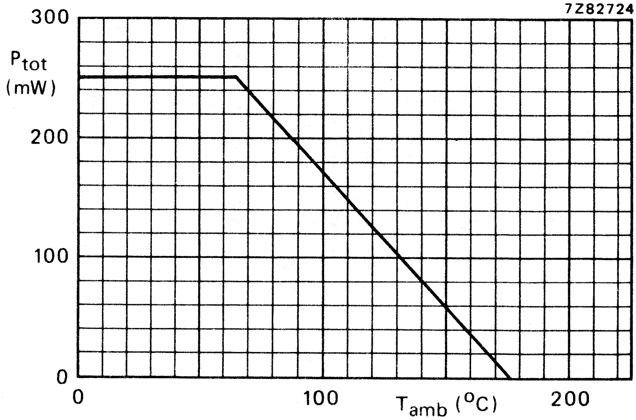


Fig. 5 Power derating curve.

N-CHANNEL FETS

Silicon symmetrical n-channel junction field-effect transistors in TO-18 metal envelopes with the gate connected to the case. The transistors are intended for switching applications. The devices have the feature: low 'on' resistance at zero gate voltage.

QUICK REFERENCE DATA

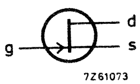
			BSV78	BSV79	BSV80	
Drain-source voltage	± V_{DS}	max.	40			V
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	350			mW
Drain current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	50	20	10	mA
Gate-source cut-off voltage I_D = 1 nA; V_{GS} = 15 V	$-V_{(P)GS}$	>	3,75	2,0	1,0	V
		<	11	7,0	5,0	V
Drain-source resistance (on) at f = 1 kHz I_D = 0; V_{GS} = 0	$r_{ds\ on}$	<	25	40	60	Ω
Feedback capacitance at f = 1 MHz V_{DS} = 0; $-V_{GS}$ = 10 V	C_{rs}	<	5	5	5	pF
Turn-on time	t_{on}	<	10	18	30	ns
Turn-off time	t_{off}	<	10	16	32	ns

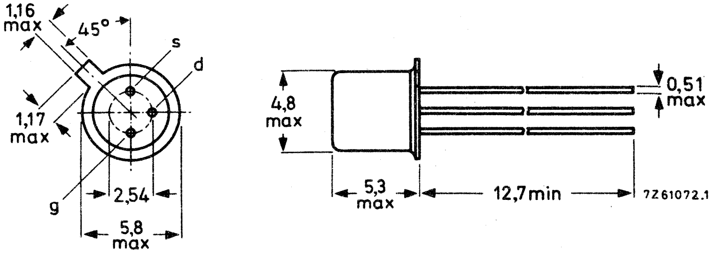
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-18.

Gate connected to case





Accessories: 56246 (distance disc).

Products approved to CECC 50 012-011, available on request.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	40	V
Drain-gate voltage (open source)	V_{DGO}	max.	40	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	40	V
Forward gate current	I_G	max.	50	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	350	mW
Storage temperature	T_{stg}	−65 to +	200	°C
Operating junction temperature	T_j	max.	175	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\,j\text{-}a}$	=	430	K/W

CHARACTERISTICS

$T_j = 25\ ^{o}C$ unless otherwise specified

Gate cut-off current				
$-V_{GS} = 20$ V; $V_{DS} = 0$	$-I_{GSS}$	<	0.25	nA
$-V_{GS} = 20$ V; $V_{DS} = 0$; $T_j = 150\ ^{o}C$	$-I_{GSS}$	<	0.5	µA
Drain cut-off current				
$V_{DS} = 15$ V; $-V_{GS} = 12$ V	I_{DSX}	<	0.25	nA
$V_{DS} = 15$ V; $-V_{GS} = 12$ V; $T_j = 150\ ^{o}C$	I_{DSX}	<	0.5	µA

			BSV78	BSV79	BSV80	
Drain current						
$V_{DS} = 15$ V; $V_{GS} = 0$	I_{DSS}	>	50	20	10	mA
Gate-source cut-off voltage						
$I_D = 1$ nA; $V_{DS} = 15$ V	$-V_{(P)GS}$	>	3.75	2.0	1.0	V
		<	11	7.0	5.0	V
Gate-source voltage						
$I_D = 1.5$ µA; $V_{DS} = 15$ V	$-V_{GS}$	>	3.5	1.75	0.75	V
		<	10	6.0	4.0	V
Drain-source voltage (on)						
$I_D = 20$ mA; $V_{GS} = 0$	V_{DSon}	<	500			mV
$I_D = 10$ mA; $V_{GS} = 0$	V_{DSon}	<		400		mV
$I_D = 5$ mA; $V_{GS} = 0$	V_{DSon}	<			325	mV
Drain-source resistance (on) at f = 1 kHz						
$I_D = 0$; $V_{GS} = 0$	$r_{ds\ on}$	<	25	40	60	Ω
y parameters at f = 1 MHz (common source)						
$-V_{GS} = 10$ V; $V_{DS} = 0$						
Input capacitance	C_{is}	<	10	10	10	pF
Feedback capacitance	C_{rs}	<	5	5	5	pF

Switching times (see Fig. 2)

Turn-on time when switched from

$-V_{GSMoff}$ = 11 V to I_{Don} = 20 mA; V_{DD} = 10 V **(BSV78)**
$-V_{GSMoff}$ = 7 V to I_{Don} = 10 mA; V_{DD} = 10 V **(BSV79)**
$-V_{GSMoff}$ = 5 V to I_{Don} = 5 mA; V_{DD} = 10 V **(BSV80)**

			BSV78	**BSV79**	**BSV80**	
delay time	t_d	<	5	10	10	ns
rise time	t_r	<	5	8	20	ns
turn-on time	t_{on}	<	10	18	30	ns

Turn-off time when switched from

I_{Don} = 20 mA to $-V_{GSMoff}$ = 11 V; V_{DD} = 10 V **(BSV78)**
I_{Don} = 10 mA to $-V_{GSMoff}$ = 7 V; V_{DD} = 10 V **(BSV79)**
I_{Don} = 5 mA to $-V_{GSMoff}$ = 5 V; V_{DD} = 10 V **(BSV80)**

			BSV78	**BSV79**	**BSV80**	
fall time	t_f	<	6	11	24	ns
storage time	t_s	<	4	5	8	ns
turn-off time	t_{off}	<	10	16	32	ns

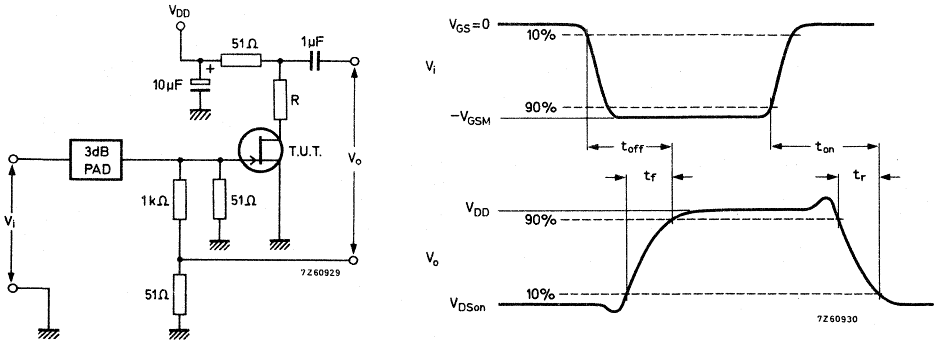


Fig. 2 Switching times test circuit and input and output waveforms.

$$R = \frac{10 - V_{DSon}\,(V)}{I_{Don}\,(A)} - 51$$

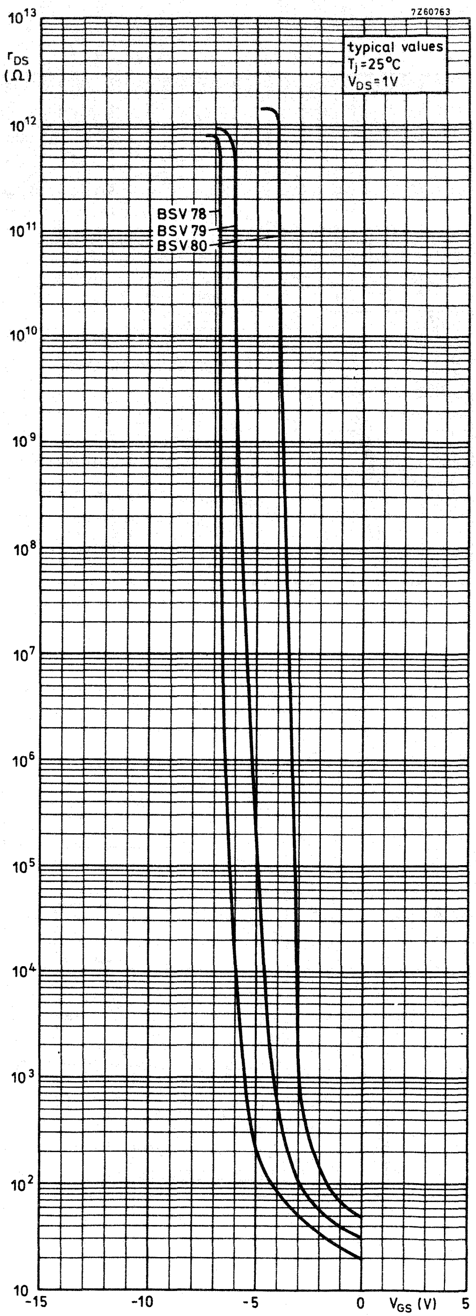
		BSV78	**BSV79**	**BSV80**
R	=	424	909	1885 Ω

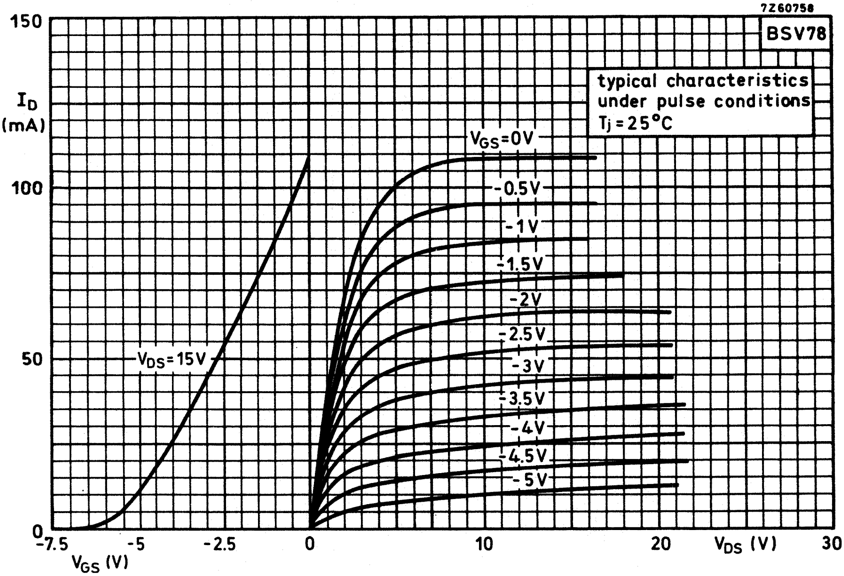
Pulse generator:

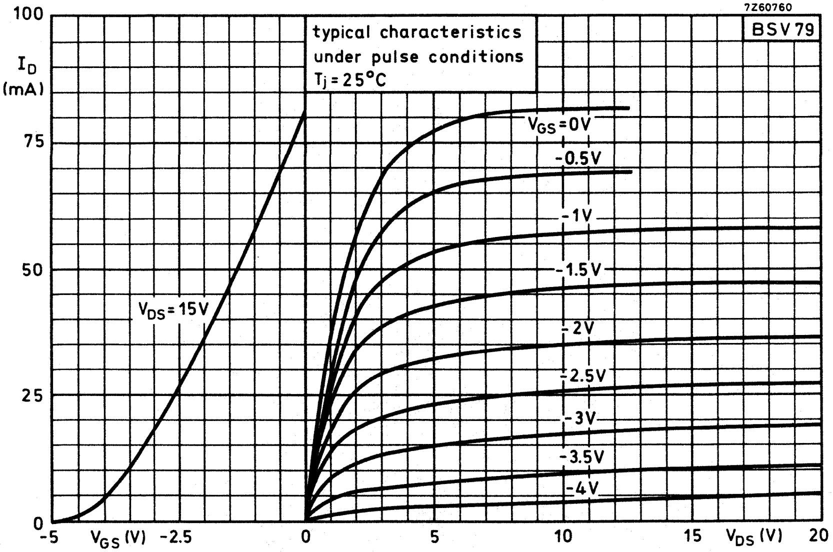
R_i = 50 Ω
t_r < 0,5 ns
t_f < 5 ns

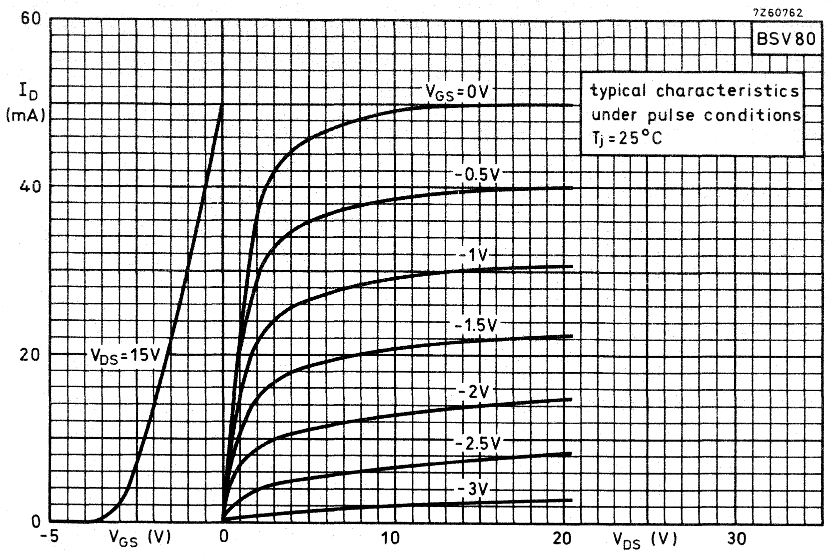
Oscilloscope:

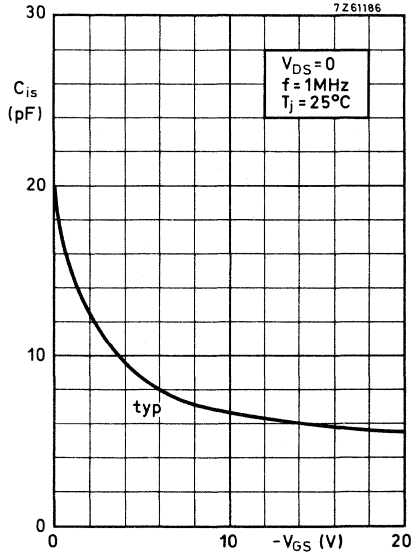
R_i = 50 Ω
t_r < 1 ns
t_f < 1 ns

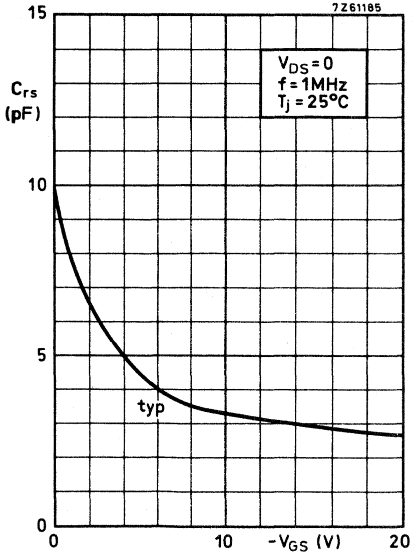

7Z60763
typical values
$T_j = 25\,°C$
$V_{DS} = 1\,V$
r_{DS} (Ω)
10^{13}
10^{12}
10^{11}
10^{10}
10^{9}
10^{8}
10^{7}
10^{6}
10^{5}
10^{4}
10^{3}
10^{2}
10
BSV 78
BSV 79
BSV 80
−15
−10
−5
0
V_{GS} (V)
5

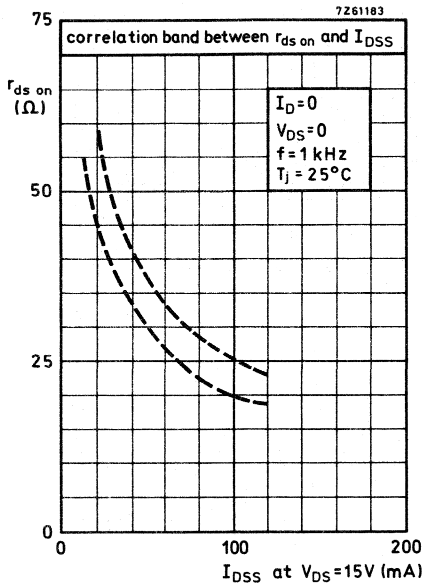

7Z60758
BSV78
typical characteristics
under pulse conditions
Tj = 25°C
150
I_D
(mA)
100
50
0
-7.5
-5
-2.5
0
10
20
30
V_GS (V)
V_DS (V)
V_DS = 15 V
V_GS = 0 V
-0.5 V
-1 V
-1.5 V
-2 V
-2.5 V
-3 V
-3.5 V
-4 V
-4.5 V
-5 V

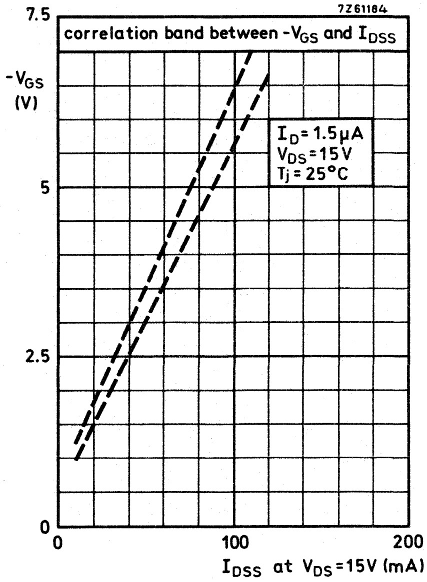

7Z60760
BSV79
typical characteristics
under pulse conditions
Tj = 25°C
100
I_D
(mA)
75
50
25
0
-5
-2.5
0
5
10
15
20
V_GS (V)
V_DS (V)
V_DS = 15 V
V_GS = 0 V
-0.5 V
-1 V
-1.5 V
-2 V
-2.5 V
-3 V
-3.5 V
-4 V


7Z60762
BSV80
typical characteristics
under pulse conditions
$T_j = 25$ °C
I_D (mA)
60
40
20
0
-5
V_{GS} (V)
0
10
20
V_{DS} (V)
30
$V_{DS} = 15$ V
$V_{GS} = 0$ V
-0.5V
-1V
-1.5V
-2V
-2.5V
-3V


7Z61186
$V_{DS} = 0$
f = 1MHz
$T_j = 25$°C
C_{is} (pF)
30
20
10
0
typ
0
10
$-V_{GS}$ (V)
20


7Z61185
$V_{DS} = 0$
f = 1MHz
$T_j = 25$°C
C_{rs} (pF)
15
10
5
0
typ
0
10
$-V_{GS}$ (V)
20


7Z61183
correlation band between $r_{ds\,on}$ and I_{DSS}
$r_{ds\,on}$
(Ω)
75
50
25
0
$I_D = 0$
$V_{DS} = 0$
f = 1 kHz
$T_j = 25$°C
0
100
200
I_{DSS} at $V_{DS} = 15$ V (mA)


7Z61184
correlation band between $-V_{GS}$ and I_{DSS}
$-V_{GS}$
(V)
7.5
5
2.5
0
$I_D = 1.5\,\mu A$
$V_{DS} = 15$ V
$T_j = 25$°C
0
100
200
I_{DSS} at $V_{DS} = 15$ V (mA)

N-CHANNEL JUNCTION FIELD-EFFECT TRANSISTOR

Symmetrical n-channel, depletion type, silicon junction field-effect transistor, designed primarily for small-signal general purpose high-frequency amplifier applications. The 2N3822 features low gate leakage current and low input capacitance.

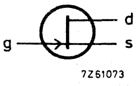
QUICK REFERENCE DATA

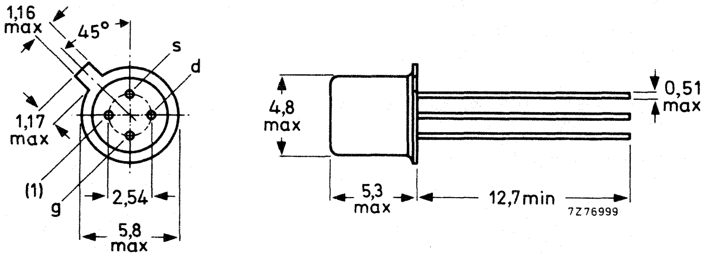
Drain-source voltage	$\pm V_{DS}$	max.	50	V
Gate-source voltage	$-V_{GS}$	max.	50	V
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300	mW
Drain current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}		2 to 10	mA
Transfer admittance (common source) V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz	$\|y_{fs}\|$		3,0 to 6,5	mA/V
V_{DS} = 15 V; V_{GS} = 0; f = 100 MHz	$\|y_{fs}\|$	>	3,0	mA/V

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-72.





(1) Shield lead connected to case.

Accessories: 56246 (distance disc).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	50	V
Drain-gate voltage	V_{DG}	max.	50	V
Gate-source voltage	$-V_{GS}$	max.	50	V
Gate current (d.c.)	I_G	max.	10	mA
Total power dissipation up to $T_{amb} = 25\ ^oC$	P_{tot}	max.	300	mW
Storage temperature	T_{stg}		−65 to + 200	°C
Junction temperature	T_j	max.	200	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	590	K/W

CHARACTERISTICS with source connected to case for all measurements

$T_{amb} = 25\ ^oC$ unless otherwise specified

Gate cut-off current				
$-V_{GS} = 30$ V; $V_{DS} = 0$	$-I_{GSS}$	<	0,1	nA
$-V_{GS} = 30$ V; $V_{DS} = 0$; $T_{amb} = 150\ ^oC$	$-I_{GSS}$	<	0,1	μA
Drain current *				
$V_{DS} = 15$ V; $V_{GS} = 0$	I_{DSS}		2 to 10	mA
Gate-source breakdown voltage				
$-I_G = 1\ \mu A$; $V_{DS} = 0$	$-V_{(BR)GSS}$	>	50	V
Gate-source voltage				
$V_{DS} = 15$ V; $I_D = 200\ \mu A$	$-V_{GS}$		1 to 4	V
Gate-source cut-off voltage				
$V_{DS} = 15$ V; $I_D = 0{,}5$ nA	$-V_{(P)GS}$	<	6	V

Small-signal common source characteristics

$V_{DS} = 15$ V; $V_{GS} = 0$

Transfer admittance *				
f = 1 kHz	$\lvert y_{fs} \rvert$		3,0 to 6,5	mA/V
f = 100 MHz	$\lvert y_{fs} \rvert$	>	3,0	mA/V
Output admittance at f = 1 kHz *	$\lvert y_{os} \rvert$	<	20	μA/V
Input capacitance at f = 1 MHz	C_{is}	<	6	pF
Feedback capacitance at f = 1 MHz	C_{rs}	<	3	pF
Noise figure				
$V_{DS} = 15$ V; $V_{GS} = 0$; $R_G = 1\ M\Omega$				
f = 10 Hz; B = 5 Hz	F	<	5	dB
Equivalent input noise voltage				
$V_{DS} = 15$ V; $V_{GS} = 0$				
f = 10 Hz; B = 5 Hz	V_n	<	200	$nV/\sqrt{Hz}$

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* Measured under pulse conditions: $t_p = 100$ ms; $\delta \leqslant 0{,}1$.

N-CHANNEL JUNCTION FIELD-EFFECT TRANSISTOR

Symmetrical n-channel, depletion type, silicon planar epitaxial junction field-effect transistor in a TO-72 metal envelope, intended for v.h.f. amplifier and mixer applications in industrial service.

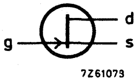
QUICK REFERENCE DATA

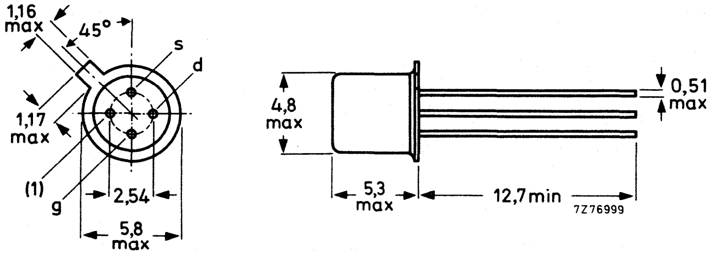
Drain-source voltage	$\pm V_{DS}$	max.	30	V
Gate-source voltage	$-V_{GS}$	max.	30	V
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300	mW
Drain current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}		4 to 20	mA
Feedback capacitance at f = 1 MHz V_{DS} = 15 V; V_{GS} = 0	C_{rs}	<	2	pF
Transfer admittance (common source) V_{DS} = 15 V; V_{GS} = 0; f = 200 MHz	$\lvert y_{fs} \rvert$	>	3,2	mA/V
Noise figure at f = 100 MHz V_{DS} = 15 V; V_{GS} = 0; R_G = 1 kΩ	F	<	2,5	dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-72.





(1) Shield lead connected to case.

Accessories: 56246 (distance disc).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage	V_{DG}	max.	30	V
Gate-source voltage	$-V_{GS}$	max.	30	V
Gate current (d.c.)	I_G	max.	10	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300	mW
Storage temperature	T_{stg}		−65 to + 200	°C
Junction temperature	T_j	max.	200	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	590	K/W

CHARACTERISTICS with source and shield connected to case for all measurements

T_{amb} = 25 °C unless otherwise specified

Gate cut-off current				
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	<	0,5	nA
$-V_{GS}$ = 20 V; V_{DS} = 0; T_{amb} = 150 °C	$-I_{GSS}$	<	0,5	μA
Drain current *				
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}		4 to 20	mA
Gate-source breakdown voltage				
$-I_G$ = 1 μA; V_{DS} = 0	$-V_{(BR)GSS}$	>	30	V
Gate-source voltage				
I_D = 400 μA; V_{DS} = 15 V	$-V_{GS}$		1,0 to 7,5	V
Gate-source cut-off voltage				
V_{DS} = 15 V; I_D = 0,5 nA	$-V_{(P)GS}$	<	8	V

Small-signal common source characteristics

V_{DS} = 15 V; V_{GS} = 0

Transfer admittance *				
f = 1 kHz	$\lvert y_{fs} \rvert$		3,5 to 6,5	mA/V
f = 200 MHz	$\lvert y_{fs} \rvert$	>	3,2	mA/V
Output admittance at f = 1 kHz *	$\lvert y_{os} \rvert$	<	35	μA/V
Input capacitance at f = 1 MHz	C_{is}	<	6	pF
Feedback capacitance at f = 1 MHz	C_{rs}	<	2	pF
Real part of input conductance at f = 200 MHz	$Re(y_{is})$	<	0,8	mA/V
Real part of output conductance at f = 200 MHz	$Re(y_{os})$	<	0,2	mA/V
Noise figure at f = 100 MHz				
V_{DS} = 15 V; V_{GS} = 0; R_G = 1 kΩ	F	<	2,5	dB

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* Measured under pulse conditions: t_p = 100 ms; $\delta \leqslant 0{,}1$.

N-CHANNEL SILICON FET

Symmetrical n-channel planar epitaxial junction field-effect transistor in a TO-72 metal envelope with the shield lead connected to the case. The transistor is suitable in a variety of low power switching applications, e.g. in multiplexing systems.

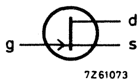
QUICK REFERENCE DATA

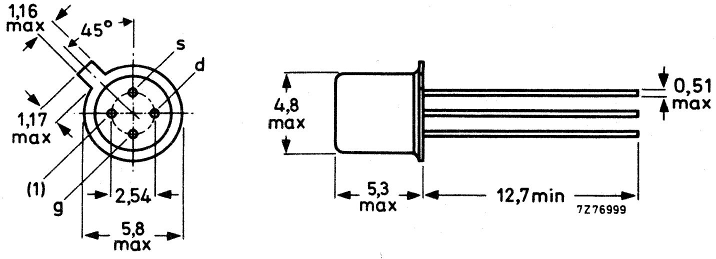
Drain-source voltage	$\pm V_{DS}$	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300	mW
Drain current V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	>	2	mA
Gate-source cut-off voltage I_D = 10 nA; V_{DS} = 10 V	$-V_{(P)GS}$		4 to 6	V
Feedback capacitance at f = 1 MHz V_{DS} = 0; V_{GS} = 7 V	C_{rs}	<	1,5	pF
Drain-source resistance (on) at f = 1 kHz V_{GS} = 0; I_D = 0	$r_{ds\ on}$	<	220	Ω

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-72.





(1) = shield lead connected to case

Accessories: 56246 (distance disc).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages				
Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Current				
Gate current	I_G	max.	10	mA
Power dissipation				
Total power dissipation up to $T_{amb} = 25\ ^{o}C$	P_{tot}	max.	300	mW
Temperatures				
Storage temperature	T_{stg}	−55 to +200		^{o}C
Junction temperature	T_j	max.	200	^{o}C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j-a}$ = 0.59 $^{o}C/mW$

CHARACTERISTICS $T_j = 25\ ^oC$ unless otherwise specified

Gate cut-off current				
$-V_{GS} = 20$ V; $V_{DS} = 0$	$-I_{GSS}$	$<$	0.1	nA
Drain current				
$V_{DG} = 20$ V; $I_S = 0$	I_{DGO}	$<$	0.1	nA
$V_{DG} = 20$ V; $I_S = 0$; $T_{amb} = 150\ ^oC$	I_{DGO}	$<$	0.2	µA
Drain current [1])				
$V_{DS} = 20$ V; $V_{GS} = 0$	I_{DSS}	$>$	2	mA
Gate-source breakdown voltage				
$-I_G = 1.0$ µA; $V_{DS} = 0$	$-V_{(BR)GS}$	$>$	30	V
Gate-source voltage				
$I_D = 10$ nA; $V_{DS} = 10$ V	$-V_{(P)GS}$		4 to 6	V
Drain-source voltage				
$I_D = 1.0$ mA; $V_{GS} = 0$	V_{DS}	$<$	0.25	V
Drain cut-off current				
$V_{DS} = 10$ V; $-V_{GS} = 7.0$ V	I_D	$<$	1.0	nA
$V_{DS} = 10$ V; $-V_{GS} = 7.0$ V; $T_{amb} = 150\ ^oC$	I_D	$<$	2.0	µA
Drain-source resistance (on) at f = 1 kHz				
$V_{GS} = 0$; $I_D = 0$	$r_{ds\ on}$	$<$	220	Ω
Input capacitance at f = 1 MHz				
$V_{DS} = 20$ V; $V_{GS} = 0$	C_{is}	$<$	6	pF
Feedback capacitance at f = 1 MHz				
$V_{DS} = 0$; $V_{GS} = 7$ V	C_{rs}	$<$	1.5	pF

CHARACTERISTICS (continued)

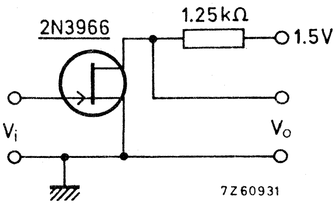
Switching times

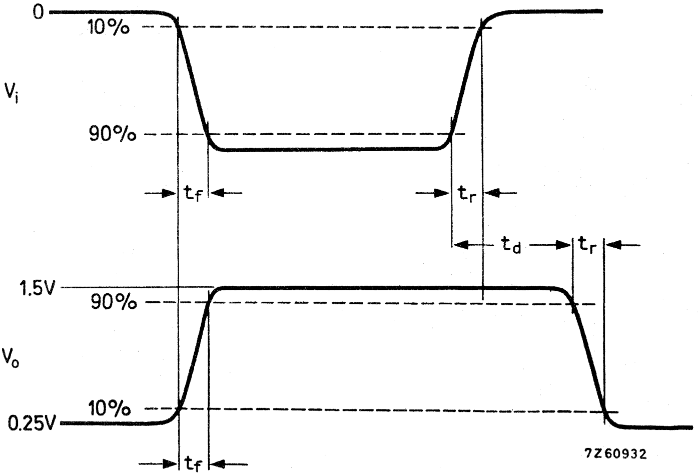
$V_{DD} = 1.5$ V; $I_{D\,on} = 1.0$ mA

$V_{GS\,on} = 0$; $-V_{GS\,off} = 6$ V

delay time	t_d	<	20	ns
rise time	t_r	<	100	ns
turn off time	t_{off}	<	100	ns

Test circuit:





Pulse generator:

t_r < 1.0 ns
t_f < 1.0 ns
t_p = 1.0 µs
δ < 0.5
R_S = 50 Ω

Oscilloscope:

t_r < 10 ns
R_i > 5 MΩ
C_i < 10 pF

N-CHANNEL FETS

Silicon symmetrical n-channel depletion type junction field-effect transistors in TO-18 metal envelopes with the gate connected to the case. The transistors are intended for low power switching applications in industrial service.

QUICK REFERENCE DATA

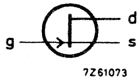
			2N4091	2N4092	2N4093	
Drain-source voltage	$\pm V_{DS}$	max.	40			V
Total power dissipation up to $T_{case} = 25\ ^{o}C$	P_{tot}	max	1,8			W
Drain current $V_{DS} = 20$ V; $V_{GS} = 0$	I_{DSS}	>	30	15	8	mA
Gate-source cut-off voltage $I_D = 1$ nA; $V_{DS} = 20$ V	$-V_{(P)GS}$	> <	5,0 10	2,0 7,0	1,0 5,0	V V
Drain-source resistance (on) at f = 1 kHz $I_D = 0$; $V_{GS} = 0$	$r_{ds\ on}$	<	30	50	80	Ω
Feedback capacitance at f = 1 MHz $V_{DS} = 0$; $-V_{GS} = 20$ V	C_{rs}	<	5,0			pF
Turn-off time $V_{DD} = 3,0$ V; $V_{GS} = 0$						
$I_D = 6,6$ mA; $-V_{GSM} = 12$ V **2N4091**	t_{off}	<	40			ns
$I_D = 4,0$ mA; $-V_{GSM} = 8$ V **2N4092**	t_{off}	<	60			ns
$I_D = 2,5$ mA; $-V_{GSM} = 6$ V **2N4093**	t_{off}	<	80			ns

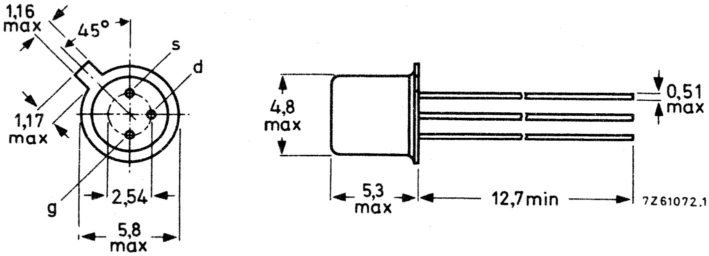
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-18.

Gate connected to case





Accessories: 56246 (distance disc).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages				
Drain-source voltage	$\pm V_{DS}$	max.	40	V
Drain-gate voltage (open source)	V_{DGO}	max.	40	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	40	V
Current				
Forward gate current (d.c.)	I_G	max.	10	mA
Power dissipation				
Total power dissipation up to T_{case} = 25 °C	P_{tot}	max.	1.8	W
Temperatures				
Storage temperature	T_{stg}	−55 to	+200	°C
Junction temperature	T_j	max.	200	°C

THERMAL RESISTANCE

From junction to case in free air	$R_{th\ j-c}$	=	0.1	°C/mW

CHARACTERISTICS $T_{amb} = 25\ ^{o}C$ unless otherwise specified

Drain current				
$V_{DG} = 20$ V; $I_S = 0$	I_{DGO}	<	0.2	nA
$V_{DG} = 20$ V; $I_S = 0$; $T_{amb} = 150\ ^{o}C$	I_{DGO}	<	0.4	μA
Source current				
$V_{SG} = 20$ V; $I_D = 0$	I_{SGO}	<	0.2	nA

			2N4091	2N4092	2N4093	
Drain cut-off current						
$V_{DS} = 20$ V; $-V_{GS} = 12$ V	I_{DSX}	<	0.2	–	–	nA
$V_{DS} = 20$ V; $-V_{GS} = 8$ V	I_{DSX}	<	–	0.2	–	nA
$V_{DS} = 20$ V; $-V_{GS} = 6$ V	I_{DSX}	<	–	–	0.2	nA
$V_{DS} = 20$ V; $-V_{GS} = 12$ V; $T_{amb} = 150\ ^{o}C$	I_{DSX}	<	0.4	–	–	μA
$V_{DS} = 20$ V; $-V_{GS} = 8$ V; $T_{amb} = 150\ ^{o}C$	I_{DSX}	<	–	0.4	–	μA
$V_{DS} = 20$ V; $-V_{GS} = 6$ V; $T_{amb} = 150\ ^{o}C$	I_{DSX}	<	–	–	0.4	μA
Gate-source breakdown voltage						
$-I_G = 1.0$ μA; $V_{DS} = 0$	$-V_{(BR)GSS}$	>	40	40	40	V
Drain current [1]						
$V_{DS} = 20$ V; $V_{GS} = 0$	I_{DSS}	>	30	15	8	mA
Gate-source cut-off voltage						
$I_D = 1$ nA; $V_{DS} = 20$ V	$-V_{(P)GS}$	>	5.0	2.0	1.0	V
		<	10	7.0	5.0	V
Drain-source voltage (on)						
$I_D = 6.6$ mA; $V_{GS} = 0$	V_{DSon}	<	0.2	–	–	V
$I_D = 4.0$ mA; $V_{GS} = 0$	V_{DSon}	<	–	0.2	–	V
$I_D = 2.5$ mA; $V_{GS} = 0$	V_{DSon}	<	–	–	0.2	V
Drain- source resistance (on)						
$I_D = 1.0$ mA; $V_{GS} = 0$	r_{DSon}	<	30	50	80	Ω
Drain-source resistance (on) at f = 1 kHz						
$I_D = 0$; $V_{GS} = 0$	$r_{ds\ on}$	<	30	50	80	Ω

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[1] Measured under pulsed conditions: $t_p \leq 300$ μs; $\delta \leq 0.03$

CHARACTERISTICS (continued) T_{amb} = 25 °C unless otherwise specified

y-parameters at f = 1 MHz (common source)

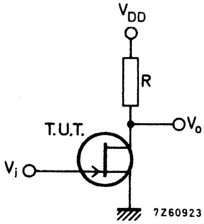
Input capacitance				
V_{DS} = 20 V ; V_{GS} = 0	C_{is}	<	16	pF
Feedback capacitance				
V_{DS} = 0 ; $-V_{GS}$ = 20 V	C_{rs}	<	5	pF

Switching times

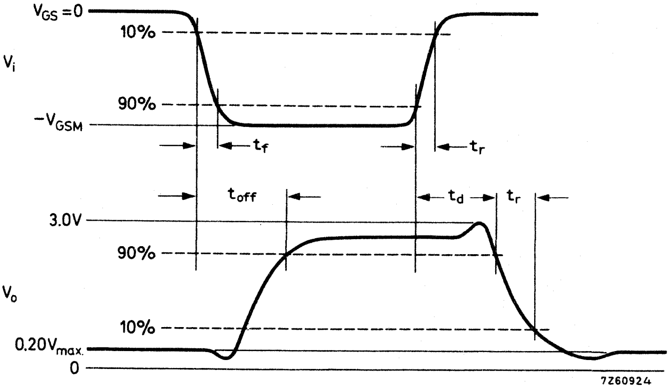
V_{DD} = 3,0 V; V_{GS} = 0

			2N4091	2N4092	2N4093	
	I_D	=	6,6	4,0	2,5	mA
	$-V_{GSM}$	=	12	8	6	V
Delay time	t_d	<	15	15	20	ns
Rise time	t_r	<	10	20	40	ns
Turn-off time	t_{off}	<	40	60	80	ns

Test circuit:



$R = \frac{2,8}{I_D}$



Pulse generator:

t_r	<	1	ns
t_f	<	1	ns
t_p	=	1,0	µs
δ	=	0,1	
R_S	=	50	Ω

Oscilloscope:

t_r	<	0,4	ns
R_i	>	9,8	MΩ
C_i	<	1,7	pF

N-CHANNEL FETS

Silicon symmetrical n-channel depletion type junction field-effect transistors in TO-18 metal envelopes with the gate connected to the case. The transistors are intended for low power, chopper or switching, application in industrial service.

QUICK REFERENCE DATA

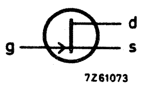
Drain-source voltage	$\pm V_{DS}$	max.		40		V
Total power dissipation up to T_{case} = 25 °C	P_{tot}	max.		1,8		W
Drain current			2N4391	2N4392	2N4393	
V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	>	50	25	5	mA
Gate-source cut-off voltage I_D = 1 nA; V_{DS} = 20 V	$-V_{(P)GS}$	>	4,0	2,0	0,5	V
		<	10	5,0	3,0	V
Drain-source resistance (on) at f = 1 kHz I_D = 1 mA; V_{GS} = 0	$r_{ds\,on}$	<	30	60	100	Ω
Feedback capacitance at f = 1 MHz V_{DS} = 0; $-V_{GS}$ = 12 V 2N4391 V_{DS} = 0; $-V_{GS}$ = 7 V 2N4392 V_{DS} = 0; $-V_{GS}$ = 5 V 2N4393	C_{rs}	<	3,5	3,5	3,5	pF
Turn-off time V_{DD} = 10 V; V_{GS} = 0						
I_D = 12 mA; $-V_{GSM}$ = 12 V	t_{off}	<	20	–	–	ns
I_D = 6,0 mA; $-V_{GSM}$ = 7 V	t_{off}	<	–	35	–	ns
I_D = 3,0 mA; $-V_{GSM}$ = 5 V	t_{off}	<	–	–	50	ns

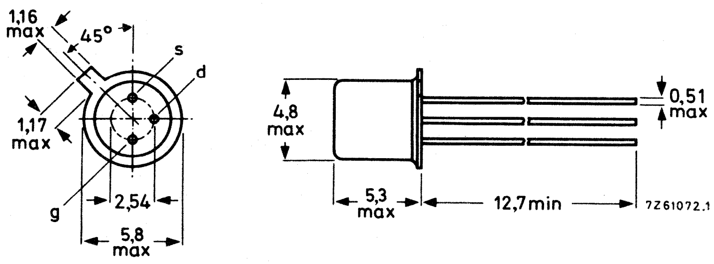
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-18.

Gate connected to case





Accessories: 56246 (distance disc).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages

Drain-source voltage	$\pm V_{DS}$	max.	40	V
Drain-gate voltage (open source)	V_{DGO}	max.	40	V
Gate-source voltage	$-V_{GSO}$	max.	40	V

Current

Gate current (d.c.)	I_G	max.	50	mA

Power dissipation

Total power dissipation up to $T_{case} = 25\ ^oC$	P_{tot}	max.	1.8	W

Temperatures

Storage temperature	T_{stg}	−65 to	200	^oC
Junction temperature	T_j	max.	200	^oC

Thermal resistance

From junction to case in free air	$R_{th\ j\text{-}c}$	=	0.1	$^oC/mW$

CHARACTERISTICS $T_{amb} = 25\ ^oC$ unless otherwise specified

Gate cut-off current

$-V_{GS} = 20$ V; $V_{DS} = 0$	$-I_{GSS} <$	0.1	nA
$-V_{GS} = 20$ V; $V_{DS} = 0$; $T_{amb} = 150\ ^oC$	$-I_{GSS} <$	0.2	μA

Drain cut-off current

		2N4391	2N4392	2N4393	
$V_{DS} = 20$ V; $-V_{GS} = 12$ V	$I_{DSX} <$	0.1	–	–	nA
$V_{DS} = 20$ V; $-V_{GS} = 7$ V	$I_{DSX} <$	–	0.1	–	nA
$V_{DS} = 20$ V; $-V_{GS} = 5$ V	$I_{DSX} <$	–	–	0.1	nA
$V_{DS} = 20$ V; $-V_{GS} = 12$ V; $T_{amb} = 150\ ^oC$	$I_{DSX} <$	0.2	–	–	μA
$V_{DS} = 20$ V; $-V_{GS} = 7$ V; $T_{amb} = 150\ ^oC$	$I_{DSX} <$	–	0.2	–	μA
$V_{DS} = 20$ V; $-V_{GS} = 5$ V; $T_{amb} = 150\ ^oC$	$I_{DSX} <$	–	–	0.2	μA

CHARACTERISTICS (continued)

T_{amb} = 25 °C unless otherwise specified

			2N4391	2N4392	2N4393	
Drain current [1]						
V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	>	50	–	–	mA
		<	150	–	–	mA
V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	>	–	25	–	mA
		<	–	75	–	mA
V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	>	–	–	5	mA
		<	–	–	30	mA
Gate-source breakdown voltage						
$-I_G$ = 1 μA; V_{DS} = 0	$-V_{(BR)GSS}$	>	40	40	40	V
Gate-source voltage						
I_G = 1 mA; V_{DS} = 0	V_{GSon}	<	1.0	1.0	1.0	V
Gate-source cut-off voltage						
I_D = 1 nA; V_{DS} = 20 V	$-V_{(P)GS}$	>	4.0	2.0	0.5	V
		<	10	5.0	3.0	V
Drain-source voltage (on)						
I_D = 12 mA; V_{GS} = 0	V_{DSon}	<	0.4	–	–	V
I_D = 6.0 mA; V_{GS} = 0	V_{DSon}	<	–	0.4	–	V
I_D = 3.0 mA; V_{GS} = 0	V_{DSon}	<	–	–	0.4	V
Drain-source resistance (on)						
I_D = 1 mA; V_{GS} = 0	r_{DSon}	<	30	60	100	Ω
Drain-source resistance (on) at f = 1 kHz						
I_D = 0; V_{GS} = 0	r_{dson}	<	30	60	100	Ω
y parameters at f = 1 MHz (common source)						
Input capacitance						
V_{DS} = 20 V; V_{GS} = 0	C_{is}	<	14	14	14	pF
Feedback capacitance						
$-V_{GS}$ = 12 V; V_{DS} = 0	C_{rs}	<	3.5	–	–	pF
$-V_{GS}$ = 7 V; V_{DS} = 0	C_{rs}	<	–	3.5	–	pF
$-V_{GS}$ = 5 V; V_{DS} = 0	C_{rs}	<	–	–	3.5	pF

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[1] measured under pulsed conditions: t_p = 100 μs; δ = 0.01

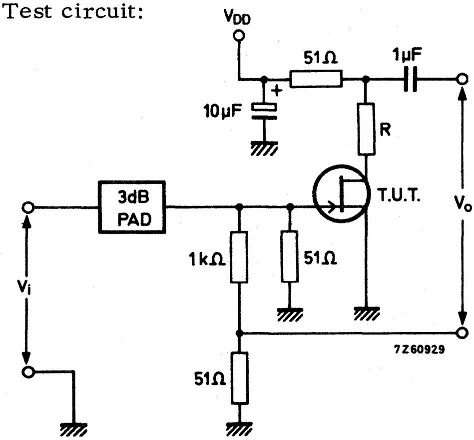
CHARACTERISTICS (continued) $T_{amb} = 25\,^{\circ}C$ unless otherwise specified

Switching times

$V_{DD} = 10\,V$; $V_{GS} = 0$

			2N4391	2N4392	2N4393	
	I_D	=	12	6.0	3.0	mA
	$-V_{GSM}$	=	12	7	5	V
Rise time	t_r	<	5	5	5	ns
Turn on time	t_{on}	<	15	15	15	ns
Fall time	t_f	<	15	20	30	ns
Turn off time	t_{off}	<	20	35	50	ns

Test circuit:



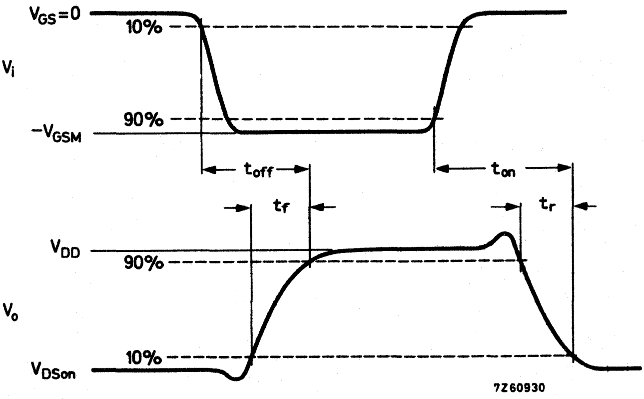
$$R = \frac{9.6}{I_D} - 51\,\Omega$$

Pulse generator:

t_r < 0.5 ns
t_f < 0.5 ns
t_p = 100 µs
δ = 0.01

Oscilloscope:

R_i = 50 Ω



N-CHANNEL FETS

Silicon symmetrical n-channel depletion type junction field-effect transistors in TO-18 metal envelopes with the gate connected to the case. The transistors are intended for low power, chopper or switching, applications in industrial service.

QUICK REFERENCE DATA

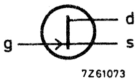
				2N4856 2N4859	2N4857 2N4860	2N4858 2N4861	
Drain-source voltage	**2N4856 to 2N4858**	$\pm V_{DS}$	max.		40		V
	2N4859 to 2N4861	$\pm V_{DS}$	max.		30		V
Total power dissipation up to T_{amb} = 25 °C		P_{tot}	max.		360		mW
Drain current V_{DS} = 15 V; V_{GS} = 0		I_{DSS}	>	50	20	8	mA
Gate-source cut-off voltage I_D = 0,5 nA; V_{DS} = 15 V		$-V_{(P)GS}$	>	4	2	0,8	V
			<	10	6	4	V
Drain-source resistance (on) at f = 1 kHz I_D = 0; V_{GS} = 0		$r_{ds\ on}$	<	25	40	60	Ω
Feedback capacitance at f = 1 MHz V_{DS} = 0; $-V_{GS}$ = 10 V		C_{rs}	<		8		pF
Turn-off time V_{DD} = 10 V; V_{GS} = 0							
I_D = 20 mA; $-V_{GSM}$ = 10 V	**2N4856; 2N4859**	t_{off}	<		25		ns
I_D = 10 mA; $-V_{GSM}$ = 6 V	**2N4857; 2N4860**	t_{off}	<		50		ns
I_D = 5 mA; $-V_{GSM}$ = 4 V	**2N4858; 2N4861**	t_{off}	<		100		ns

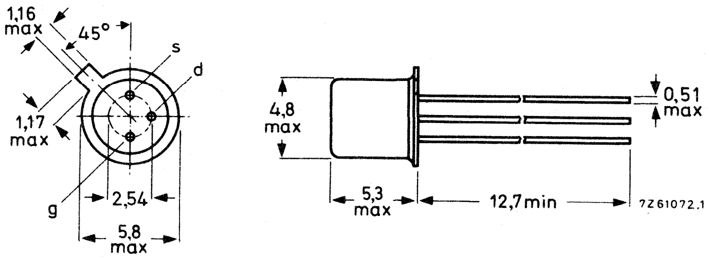
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-18

Gate connected to case





Accessories: 56246 (distance disc).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

			2N4856 2N4857 2N4858	2N4859 2N4860 2N4861	
Voltages					
Drain-source voltage	$\pm V_{DS}$	max.	40	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	40	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	40	30	V
Current					
Gate current (d.c.)	I_G	max.	50		mA
Power dissipation					
Total power dissipation up to $T_{amb} = 25\ ^{o}C$	P_{tot}	max.	360		mW
Temperatures					
Storage temperature	T_{stg}	−65 to	+200		°C
Junction temperature	T_j	max.	200		°C

THERMAL RESISTANCE

From junction to ambient in free air $R_{th\ j\text{-}a}$ = 0.49 °C/mW

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

			2N4856 2N4857 2N4858	2N4859 2N4860 2N4861	
Gate cut-off current					
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	<	0.25	–	nA
$-V_{GS}$ = 15 V; V_{DS} = 0	$-I_{GSS}$	<	–	0.25	nA
$-V_{GS}$ = 20 V; V_{DS} = 0; T_{amb} = 150 °C	$-I_{GSS}$	<	0.5	–	μA
$-V_{GS}$ = 15 V; V_{DS} = 0; T_{amb} = 150 °C	$-I_{GSS}$	<	–	0.5	μA
Drain cut-off current					
V_{DS} = 15 V; $-V_{GS}$ = 10 V	I_{DSX}	<	0.25	0.25	nA
V_{DS} = 15 V; $-V_{GS}$ = 10 V; T_{amb} = 150 °C	I_{DSX}	<	0.5	0.5	μA

			2N4856 2N4859	2N4857 2N4860	2N4858 2N4861	
Drain current [1]						
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	50	20	8	mA
	I_{DSS}	<	–	100	80	mA

		2N4856 2N4857 2N4858	2N4859 2N4860 2N4861	
Gate-source breakdown voltage				
$-I_G$ = 1 μA; V_{DS} = 0	$-V_{(BR)GSS}$	40	30	V

			2N4856 2N4859	2N4857 2N4860	2N4858 2N4861	
Gate-source cut-off voltage						
I_D = 0.5 nA; V_{DS} = 15 V	$-V_{(P)GS}$	>	4	2	0.8	V
		<	10	6	4	V
Drain-source voltage (on)						
I_D = 20 mA; V_{GS} = 0	V_{DSon}	<	0.75	–	–	V
I_D = 10 mA; V_{GS} = 0	V_{DSon}	<	–	0.50	–	V
I_D = 5 mA; V_{GS} = 0	V_{DSon}	<	–	–	0.50	V
Drain-source resistance (on) at f = 1 kHz						
I_D = 0; V_{GS} = 0	r_{dson}	<	25	40	60	Ω

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[1]) measured under pulse conditions: t_p = 100 ms; $\delta \leq 0.1$

y-parameters (common source)

$V_{DS} = 0; -V_{GS} = 10$ V; f = 1 MHz

Input capacitance	C_{is}	<	18	pF
Feedback capacitance	C_{rs}	<	8	pF

Switching times (see Figs 2 and 3)

$V_{DD} = 10$ V; $V_{GS} = 0$

			2N4856 **2N4859**	**2N4857** **2N4860**	**2N4858** **2N4861**	
Drain current	I_D	=	20	10	5	mA
Gate-source voltage (peak value)	$-V_{GSM}$	=	10	6	4	V
Delay time	t_d	<	6	6	10	ns
Rise time	t_r	<	3	4	10	ns
Turn-off time	t_{off}	<	25	50	100	ns

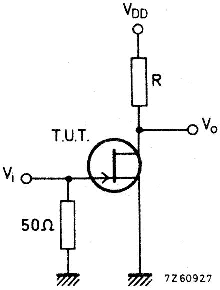


Fig. 2 Switching times test circuit.

	2N4856 **2N4859**	**2N4857** **2N4860**	**2N4858** **2N4861**	
R =	464	953	1910	Ω

Pulse generator:

$t_r \leqslant 1$ ns

$t_f \leqslant 1$ ns

$\delta = 0{,}02$

$Z_o = 50\ \Omega$

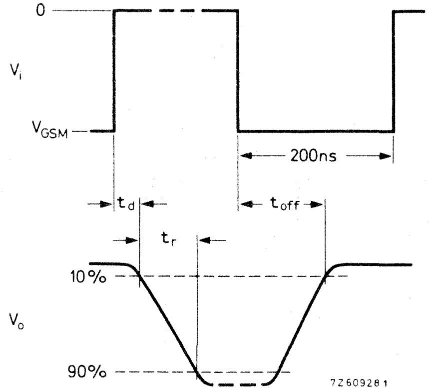


Fig. 3 Input and output waveforms.

Oscilloscope:

$t_r \leqslant 0{,}75$ ns

$R_i \geqslant 1\ M\Omega$

$C_i \leqslant 2{,}5$ pF

DEVICE DATA

MOS-FETS

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for use in u.h.f. applications in television tuners and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

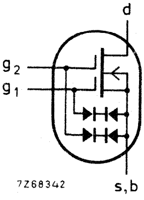
QUICK REFERENCE DATA

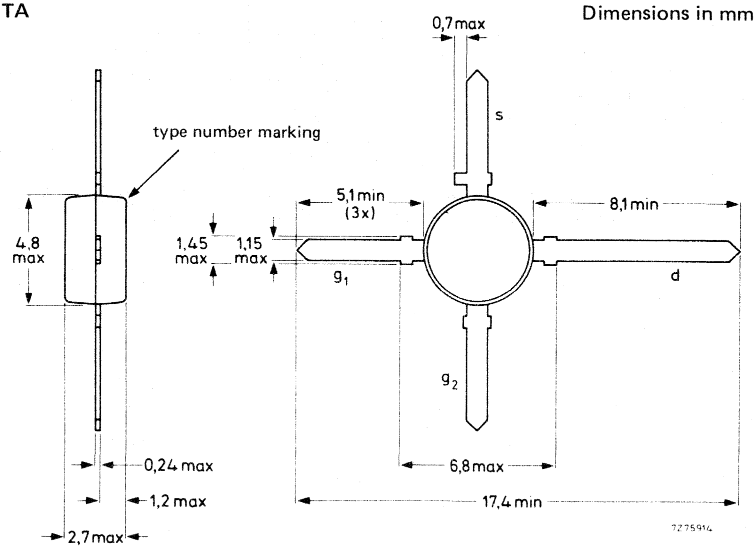
Drain-source voltage	V_{DS}	max.	20	V
Drain current (peak value)	I_{DM}	max.	30	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225	mW
Junction temperature	T_j	max.	150	°C
Transfer admittance at f = 1 kHz I_D = 7 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs} \rvert$	typ.	12	mA/V
Feedback capacitance at f = 1 MHz I_D = 7 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	25	fF
Noise figure at G_S = 2 mA/V I_D = 7 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; f = 800 MHz	F	typ.	2,8	dB
Power gain at f = 800 MHz I_D = 7 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; G_S = 2 mA/V; G_L = 1 mA/V	G_p	typ.	16,5	dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-103.





RATINGS

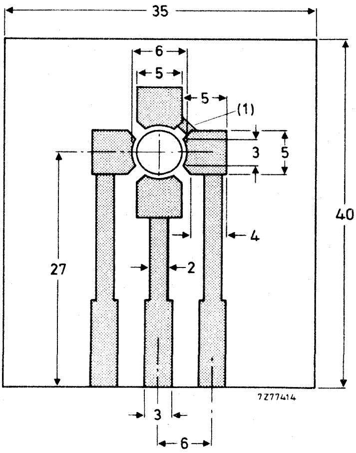
Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain current (d.c. or average)	I_D	max.	20	mA
Drain current (peak value)	I_{DM}	max.	30	mA
Gate 1 - source current	$\pm I_{G1\text{-}S}$	max.	10	mA
Gate 2 - source current	$\pm I_{G2\text{-}S}$	max.	10	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225	mW
Storage temperature	T_{stg}		−65 to +150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air mounted on the printed-circuit board	$R_{th\ j\text{-}a}$	=	335	K/W

Dimensions in mm



(1) Connection made by a strip or Cu wire.

Fig. 2 Single-sided 35 μm Cu-clad epoxy fibre-glass printed-circuit board, thickness 1,5 mm. Tracks are fully tin-lead plated. Board in horizontal position for R_{th} measurement.

STATIC CHARACTERISTICS

T_{amb} = 25 °C

Gate cut-off currents				
$\pm V_{G1\text{-}S} = 5$ V; $V_{G2\text{-}S} = V_{DS} = 0$	$\pm I_{G1\text{-}SS}$	$<$	50	nA
$\pm V_{G2\text{-}S} = 5$ V; $V_{G1\text{-}S} = V_{DS} = 0$	$\pm I_{G2\text{-}SS}$	$<$	50	nA
Gate-source breakdown voltages				
$\pm I_{G1\text{-}SS} = 10$ mA; $V_{G2\text{-}S} = V_{DS} = 0$	$\pm V_{(BR)G1\text{-}SS}$		6,0 to 20	V
$\pm I_{G2\text{-}SS} = 10$ mA; $V_{G1\text{-}S} = V_{DS} = 0$	$\pm V_{(BR)G2\text{-}SS}$		6,0 to 20	V
Drain current*				
$V_{DS} = 10$ V; $V_{G1\text{-}S} = 0$; $+V_{G2\text{-}S} = 4$ V	I_{DSS}		2 to 20	mA
Gate-source cut-off voltages				
$I_D = 20\ \mu$A; $V_{DS} = 10$ V; $+V_{G2\text{-}S} = 4$ V	$-V_{(P)G1\text{-}S}$	$<$	2,7	V
$I_D = 20\ \mu$A; $V_{DS} = 10$ V; $V_{G1\text{-}S} = 0$	$-V_{(P)G2\text{-}S}$	$<$	2,7	V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): $I_D = 7$ mA; $V_{DS} = 10$ V; $+V_{G2\text{-}S} = 4$ V; T_{amb} = 25 °C

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	$>$	9,5	mA/V
		typ.	12	mA/V
Input capacitance at gate 1; f = 1 MHz	$C_{ig1\text{-}s}$	typ.	1,8	pF
Input capacitance at gate 2; f = 1 MHz	$C_{ig2\text{-}s}$	typ.	1,0	pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25	fF
Output capacitance at f = 1 MHz	C_{os}	typ.	0,9	pF
Noise figure at $G_S = 2$ mA/V				
f = 200 MHz	F	typ.	1,6	dB
f = 800 MHz	F	typ.	2,8	dB
Power gain at $G_S = 2$ mA/V				
$G_L = 0{,}5$ mA/V; f = 200 MHz	G_p	typ.	23	dB
$G_L = 1$ mA/V; f = 800 MHz	G_p	typ.	16,5	dB

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* Measured under pulse conditions.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for v.h.f. applications in television tuners, especially in r.f. stages and mixer stages in S-channel tuners. The device is also suitable for use in professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

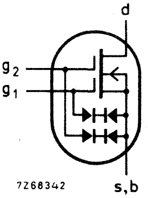
QUICK REFERENCE DATA

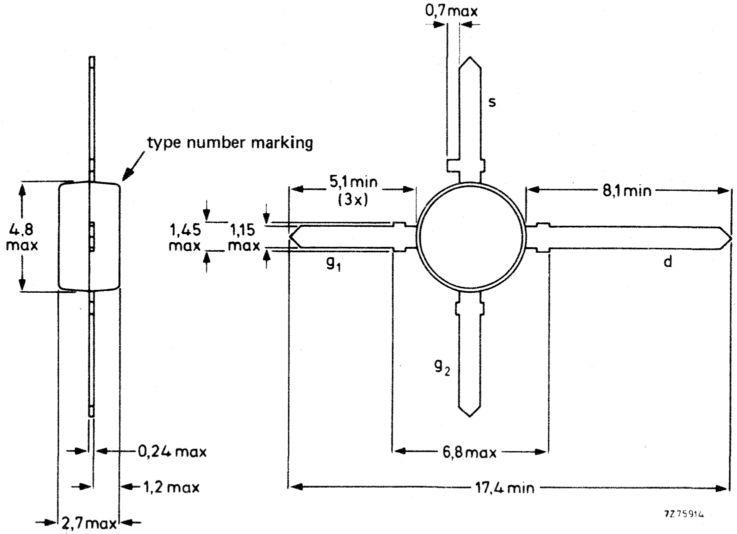
Drain-source voltage	V_{DS}	max.	20	V
Drain-current	I_D	max.	30	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225	mW
Junction temperature	T_j	max.	150	°C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 15 V; $+V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs} \rvert$	typ.	17	mA/V
Feedback capacitance at f = 1 MHz I_D = 10 mA, V_{DS} = 15 V; $+V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	25	fF
Noise figure at G_S = 2 mA/V I_D = 10 mA; V_{DS} = 15 V; $+V_{G2\text{-}S}$ = 4 V; f = 200 MHz	F	typ.	1,5	dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-103.





RATINGS

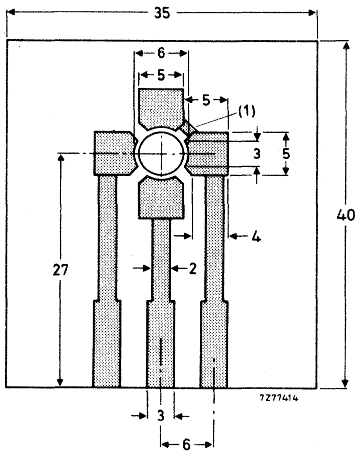
Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain-current (d.c. or average)	I_D	max.	30	mA
Gate 1 - source current	$\pm I_{G1\text{-}S}$	max.	10	mA
Gate 2 - source current	$\pm I_{G2\text{-}S}$	max.	10	mA
Total power dissipation up to $T_{amb} = 75\ ^oC$	P_{tot}	max.	225	mW
Storage temperature	T_{stg}	−65 to	+150	^oC
Junction temperature	T_j	max.	150	^oC

THERMAL RESISTANCE

From junction to ambient in free air mounted on the printed-circuit board (see Fig. 2)	$R_{th\ j\text{-}a}$	=	335	K/W

Dimensions in mm



(1) Connection made by a strip or Cu wire.

Fig. 2 Single-sided 35 μm Cu-clad epoxy fibre-glass printed-circuit board, thickness 1,5 mm. Tracks are fully tin-lead plated. Board in horizontal position for R_{th} measurement.

STATIC CHARACTERISTICS

$T_{amb} = 25\ ^{o}C$

Gate cut-off currents			
$\pm V_{G1\text{-}S} = 5$ V; $V_{G2\text{-}S} = V_{DS} = 0$	$\pm I_{G1\text{-}SS}$	$<$	50 nA
$\pm V_{G2\text{-}S} = 5$ V; $V_{G1\text{-}S} = V_{DS} = 0$	$\pm I_{G2\text{-}SS}$	$<$	50 nA
Gate-source breakdown voltages			
$\pm I_{G1\text{-}SS} = 10$ mA; $V_{G2\text{-}S} = V_{DS} = 0$	$\pm V_{(BR)G1\text{-}SS}$		6,0 to 20 V
$\pm I_{G2\text{-}SS} = 10$ mA; $V_{G1\text{-}S} = V_{DS} = 0$	$\pm V_{(BR)G2\text{-}SS}$		6,0 to 20 V
Drain current*			
$V_{DS} = 15$ V; $V_{G1\text{-}S} = 0$; $+V_{G2\text{-}S} = 4$ V	I_{DSS}		2 to 20 mA
Gate-source cut-off voltages			
$I_D = 20\ \mu$A; $V_{DS} = 15$ V; $+V_{G2\text{-}S} = 4$ V	$-V_{(P)G1\text{-}S}$	$<$	2,5 V
$I_D = 20\ \mu$A; $V_{DS} = 15$ V; $V_{G1\text{-}S} = 0$	$-V_{(P)G2\text{-}S}$	$<$	2,0 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source); $I_D = 10$ mA; $V_{DS} = 15$ V; $+V_{G2\text{-}S} = 4$ V; $T_{amb} = 25\ ^{o}C$

Transfer admittance at f = 1 kHz	$\|y_{fs}\|$	$>$ typ.	15 mA/V 17 mA/V
Input capacitance at gate 1; f = 1 MHz	$C_{ig1\text{-}s}$	typ. $<$	2,5 pF 3,0 pF
Input capacitance at gate 2; f = 1 MHz	$C_{ig2\text{-}s}$	typ.	1,2 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ. $<$	25 fF 35 fF
Output capacitance at f = 1 MHz	C_{os}	typ. $<$	1,0 pF 1,3 pF
Noise figure at $G_S = 2$ mA/V f = 200 MHz	F	typ. $<$	1,5 dB 2,8 dB
Power gain at $G_S = 2$ mA/V $G_L = 0{,}5$ mA/V; f = 200 MHz	G_p	typ.	25 dB

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* Measured under pulse conditions.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for u.h.f. applications in television tuners and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

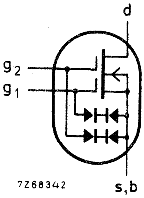
QUICK REFERENCE DATA

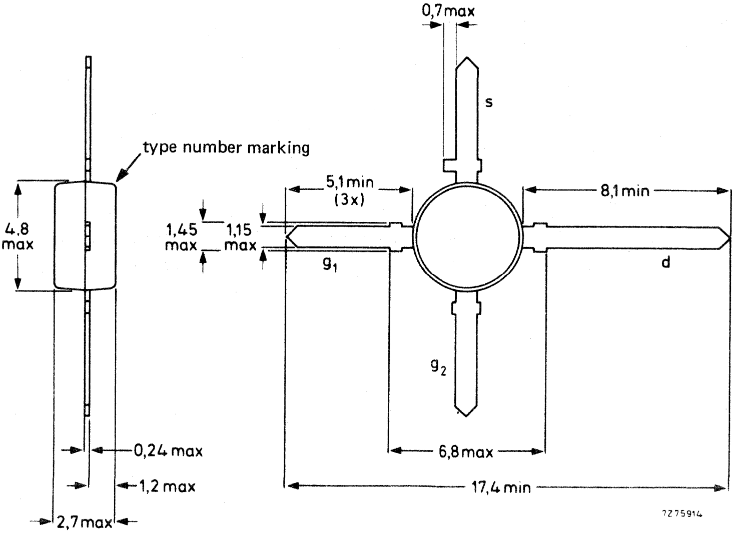
Drain-source voltage	V_{DS}	max.	20	V
Drain-current	I_D	max.	30	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225	mW
Junction temperature	T_j	max.	150	°C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 15 V; $+V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs}\rvert$	typ.	17	mA/V
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; $+V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	25	fF
Noise figure at G_S = 2 mA/V I_D = 10 mA; V_{DS} = 15 V; $+V_{G2\text{-}S}$ = 4 V; f = 800 MHz	F	typ.	2,8	dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-103.





RATINGS

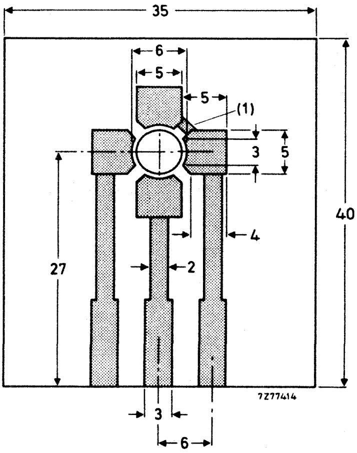
Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain source voltage	V_{DS}	max.	20	V
Drain current (d.c. or average)	I_D	max.	30	mA
Gate 1 - source current	$\pm I_{G1\text{-}S}$	max.	10	mA
Gate 2 - source current	$\pm I_{G2\text{-}S}$	max.	10	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225	mW
Storage temperature	T_{stg}	−65 to	+150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air mounted on the printed-circuit board (see Fig. 2)	$R_{th\,j\text{-}a}$	=	335	K/W

Dimensions in mm



(1) Connection made by a strip or Cu wire.

Fig. 2 Single-sided 35 μm Cu-clad epoxy fibre-glass printed-circuit board, thickness 1,5 mm. Tracks are fully tin-lead plated. Board in horizontal position for R_{th} measurement.

STATIC CHARACTERISTICS

T_{amb} = 25 °C

Gate cut-off currents			
$\pm V_{G1\text{-}S} = 5$ V; $V_{G2\text{-}S} = V_{DS} = 0$	$\pm I_{G1\text{-}SS}$	$<$	50 nA
$\pm V_{G2\text{-}S} = 5$ V; $V_{G1\text{-}S} = V_{DS} = 0$	$\pm I_{G2\text{-}SS}$	$<$	50 nA
Gate-source breakdown voltages			
$\pm I_{G1\text{-}SS} = 10$ mA; $V_{G2\text{-}S} = V_{DS} = 0$	$\pm V_{(BR)G1\text{-}SS}$		6,0 to 20 V
$\pm I_{G2\text{-}SS} = 10$ mA; $V_{G1\text{-}S} = V_{DS} = 0$	$\pm V_{(BR)G2\text{-}SS}$		6,0 to 20 V
Drain current*			
$V_{DS} = 15$ V; $V_{G1\text{-}S} = 0$; $+V_{G2\text{-}S} = 4$ V	I_{DSS}		2 to 20 mA
Gate-source cut-off voltages			
$I_D = 20\ \mu$A; $V_{DS} = 15$ V; $+V_{G2\text{-}S} = 4$ V	$-V_{(P)G1\text{-}S}$	$<$	2,5 V
$I_D = 20\ \mu$A; $V_{DS} = 15$ V; $V_{G1\text{-}S} = 0$	$-V_{(P)G2\text{-}S}$	$<$	2,0 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): $I_D = 10$ mA; $V_{DS} = 15$ V; $+V_{G2\text{-}S} = 4$ V; $T_{amb} = 25$ °C

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	$>$ typ.	15 mA/V 17 mA/V
Input capacitance at gate 1; f = 1 MHz	$C_{ig1\text{-}s}$	typ. $<$	2,2 pF 2,6 pF
Input capacitance at gate 2; f = 1 MHz	$C_{ig2\text{-}s}$	typ.	1,1 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ. $<$	25 fF 35 fF
Output capacitance at f = 1 MHz	C_{os}	typ. $<$	0,8 pF 1,2 pF
Noise figure at $G_S = 2$ mA/V			
f = 200 MHz	F	typ.	1,5 dB
f = 800 MHz	F	typ. $<$	2,8 dB 3,9 dB
Power gain at $G_S = 2$ mA/V			
$G_L = 0{,}5$ mA/V; f = 200 MHz	G_p	typ.	25 dB
$G_L = 1$ mA/V; f = 800 MHz	G_p	typ.	18 dB

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* Measured under pulse conditions.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for u.h.f. applications, such as u.h.f. television tuners, with 12 V supply voltage.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

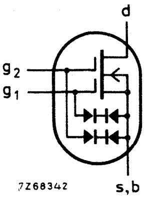
QUICK REFERENCE DATA

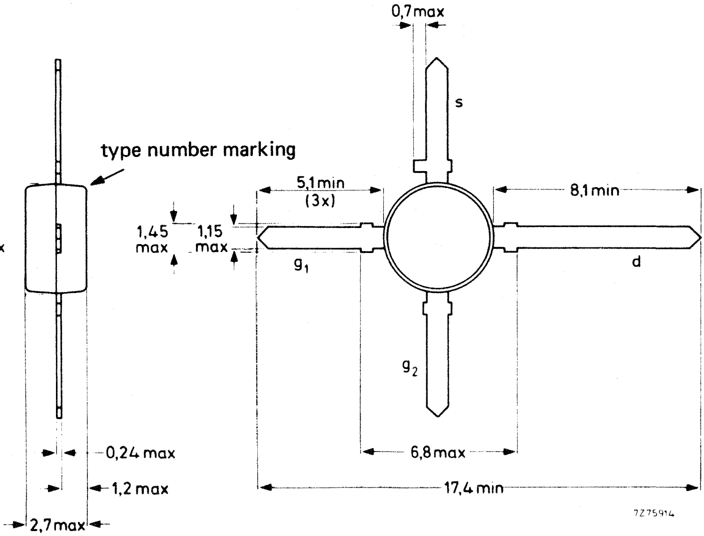
Drain-source voltage	V_{DS}	max.	18	V
Drain current	I_D	max.	30	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225	mW
Junction temperature	T_j	max.	150	°C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 10 V; $+V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs} \rvert$	typ.	19	mA/V
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; $+V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	25	fF
Noise figure at G_S = 5 mA/V I_D = 10 mA; V_{DS} = 10 V; $+V_{G2\text{-}S}$ = 4 V; f = 800 MHz	F	typ.	2,8	dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-103.





RATINGS

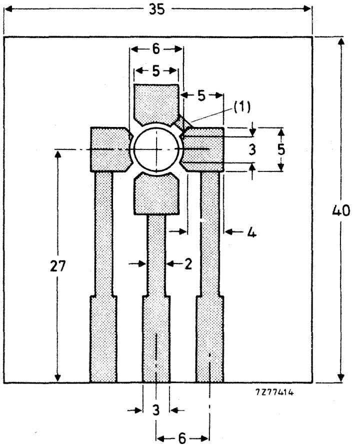
Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	18	V
Drain current (d.c. or average)	I_D	max.	30	mA
Gate 1 - source current	$\pm I_{G1\text{-}S}$	max.	10	mA
Gate 2 - source current	$\pm I_{G2\text{-}S}$	max.	10	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225	mW
Storage temperature	T_{stg}		−65 to +150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air mounted on the printed-circuit board (see Fig. 2)	$R_{th\ j\text{-}a}$	=	335	K/W

Dimensions in mm



(1) Connection made by a strip or Cu wire.

Fig. 2 Single-sided 35 μm Cu-clad epoxy fibre-glass printed-circuit board, thickness 1,5 mm. Tracks are fully tin-lead plated. Board in horizontal position for R_{th} measurement.

STATIC CHARACTERISTICS

$T_{amb} = 25\ ^oC$

Gate cut-off currents			
$\pm V_{G1\text{-}S} = 7\ V;\ V_{G2\text{-}S} = V_{DS} = 0$	$\pm I_{G1\text{-}SS}$	$<$	25 nA
$\pm V_{G2\text{-}S} = 7\ V;\ V_{G1\text{-}S} = V_{DS} = 0$	$\pm I_{G2\text{-}SS}$	$<$	25 nA
Gate-source breakdown voltages			
$\pm I_{G1\text{-}SS} = 10\ mA;\ V_{G2\text{-}S} = V_{DS} = 0$	$\pm V_{(BR)G1\text{-}SS}$	$>$	8 V
$\pm I_{G2\text{-}SS} = 10\ mA;\ V_{G1\text{-}S} = V_{DS} = 0$	$\pm V_{(BR)G2\text{-}SS}$	$>$	8 V
Gate-source cut-off voltages			
$I_D = 20\ \mu A;\ V_{DS} = 10\ V;\ +V_{G2\text{-}S} = 4\ V$	$-V_{(P)G1\text{-}S}$	$<$ $>$	1,3 V 0,2 V
$I_D = 20\ \mu A;\ V_{DS} = 10\ V;\ V_{G1\text{-}S} = 0$	$-V_{(P)G2\text{-}S}$	$<$ $>$	1,1 V 0,2 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): $I_D = 10\ mA;\ V_{DS} = 10\ V;\ +V_{G2\text{-}S} = 4\ V;\ T_{amb} = 25\ ^oC$

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	$>$ typ.	17 mA/V 19 mA/V
Input capacitance at gate 1; f = 1 MHz	$C_{ig1\text{-}s}$	$<$ typ.	3,0 pF 2,6 pF
Feedback capacitance at f = 1 MHz	C_{rs}	$<$ typ.	35 fF 25 fF
Output capacitance at f = 1 MHz	C_{os}	$<$ typ.	1,3 pF 1,1 pF
Noise figure at f = 800 MHz; $G_S = 5\ mA/V$	F	$<$ typ.	3,9 dB 2,8 dB

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for v.h.f. applications, such as v.h.f. television tuners, f.m. tuners and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

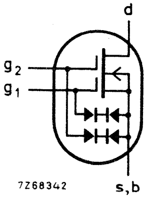
QUICK REFERENCE DATA

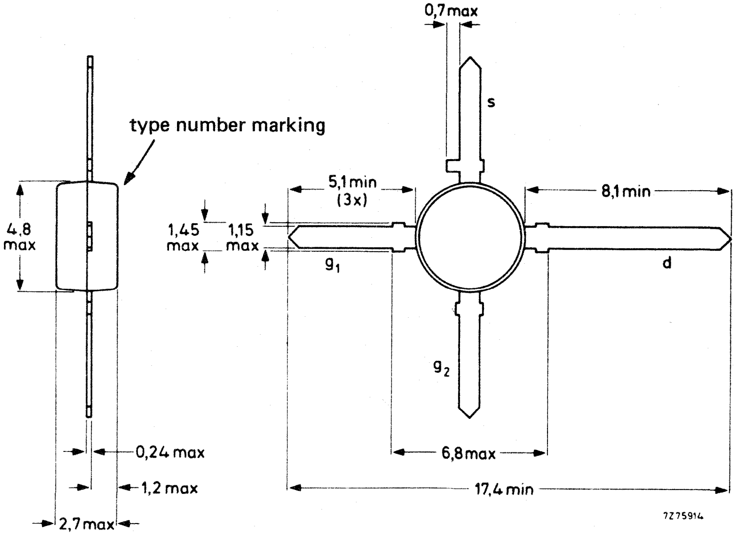
Drain-source voltage	V_{DS}	max.	20	V
Drain current	I_D	max.	20	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225	mW
Junction temperature	T_j	max.	150	°C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 10 V; $+V_{G2\text{-}S}$ = 4 V	$\|y_{fs}\|$	typ.	14	mA/V
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; $+V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	20	fF
Noise figure at optimum source admittance I_D = 10 mA; V_{DS} = 10 V; $+V_{G2\text{-}S}$ = 4 V; f = 200 MHz	F	typ.	0,7	dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-103.





RATINGS

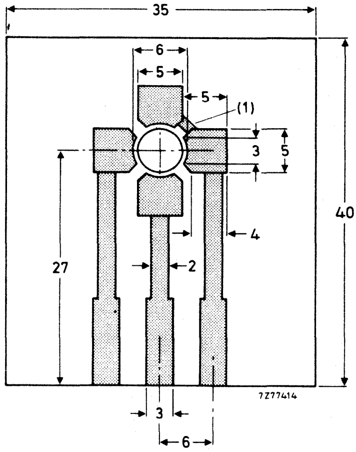
Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain current (d.c. or average)	I_D	max.	20	mA
Drain current (peak value)	I_{DM}	max.	30	mA
Gate 1 - source current	$\pm I_{G1\text{-}S}$	max.	10	mA
Gate 2 - source current	$\pm I_{G2\text{-}S}$	max.	10	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225	mW
Storage temperature	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air mounted on the printed-circuit board (see Fig. 2)	$R_{th\ j\text{-}a}$	=	335	K/W

Dimensions in mm



(1) Connection made by a strip or Cu wire.

Fig. 2 Single-sided 35 μm Cu-clad epoxy fibre-glass printed-circuit board, thickness 1,5 mm. Tracks are fully tin-lead plated. Board in horizontal position for R_{th} measurement.

STATIC CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

Gate cut-off currents				
$\pm V_{G1\text{-}S} = 5$ V; $V_{G2\text{-}S} = V_{DS} = 0$	$\pm I_{G1\text{-}SS}$	$<$	50	nA
$\pm V_{G2\text{-}S} = 5$ V; $V_{G1\text{-}S} = V_{DS} = 0$	$\pm I_{G2\text{-}SS}$	$<$	50	nA
Gate-source breakdown voltages				
$\pm I_{G1\text{-}SS} = 10$ mA; $V_{G2\text{-}S} = V_{DS} = 0$	$\pm V_{(BR)G1\text{-}SS}$	$>$	6	V
$\pm I_{G2\text{-}SS} = 10$ mA; $V_{G1\text{-}S} = V_{DS} = 0$	$\pm V_{(BR)G2\text{-}SS}$	$>$	6	V
Drain current				
$V_{DS} = 10$ V; $V_{G1\text{-}S} = 0$; $+V_{G2\text{-}S} = 4$ V; $T_j = 25$ °C	I_{DSS}		4 to 25	mA
Gate-source cut-off voltages				
$I_D = 20\ \mu$A; $V_{DS} = 10$ V; $+V_{G2\text{-}S} = 4$ V	$-V_{(P)G1\text{-}S}$	$<$	2,5	V
$I_D = 20\ \mu$A; $V_{DS} = 10$ V; $V_{G1\text{-}S} = 0$	$-V_{(P)G2\text{-}S}$	$<$	2,5	V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): $I_D = 10$ mA; $V_{DS} = 10$ V; $+V_{G2\text{-}S} = 4$ V; $T_{amb} = 25$ °C

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	$>$ typ.	10 14	mA/V mA/V
Input capacitance at gate 1; f = 1 MHz	$C_{ig1\text{-}s}$	typ.	2,1	pF
Input capacitance at gate 2; f = 1 MHz	$C_{ig2\text{-}s}$	typ.	1,0	pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	20	fF
Output capacitance at f = 1 MHz	C_{os}	typ.	1,1	pF
Noise figure at f = 100 MHz; $G_S = 1$ mA/V	F	typ. $<$	0,7 1,7	dB dB
Noise figure at f = 200 MHz; $G_S = 2$ mA/V	F	typ. $<$	1,0 2,0	dB dB
Transducer gain at f = 100 MHz; $G_S = 1$ mA/V; $G_L = 0{,}5$ mA/V	G_{tr}	typ.	29	dB
Transducer gain at f = 200 MHz; $G_S = 2$ mA/V; $G_L = 0{,}5$ mA/V	G_{tr}	typ.	26	dB

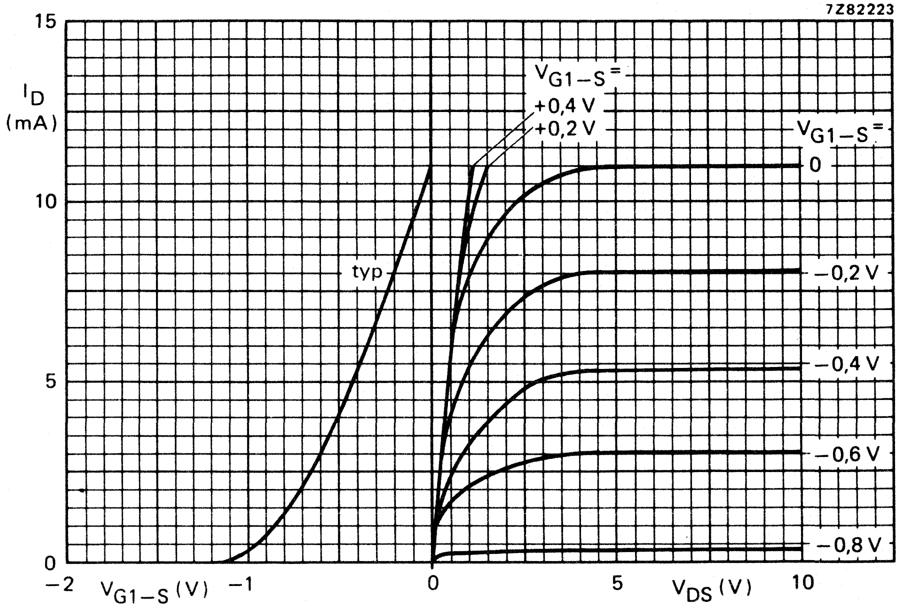


Fig. 3 **Left-hand graph:** V_{DS} = 10 V; $V_{G2\text{-}S}$ = + 4 V; T_{amb} = 25 °C. **Right-hand graph:** $V_{G2\text{-}S}$ = + 4 V; T_{amb} = 25 °C.

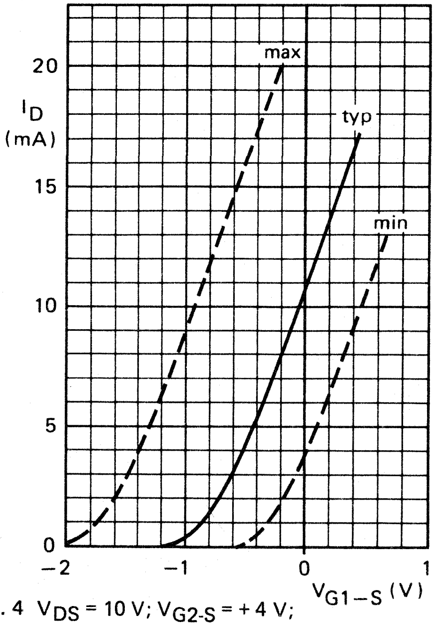


Fig. 4 V_{DS} = 10 V; $V_{G2\text{-}S}$ = + 4 V; T_{amb} = 25 °C.

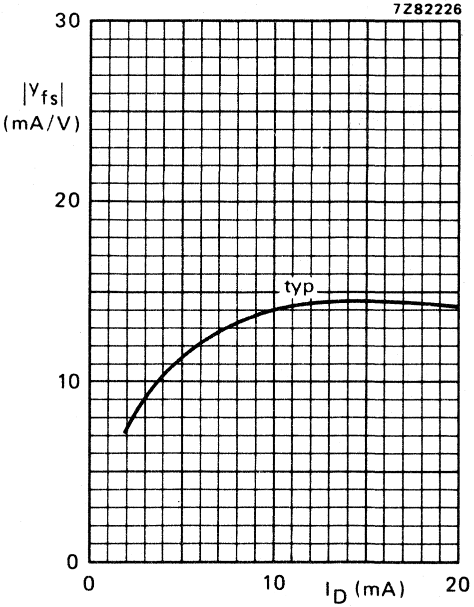


Fig. 5 V_{DS} = 10 V; $V_{G2\text{-}S}$ = + 4 V; f = 1 kHz; T_{amb} = 25 °C.

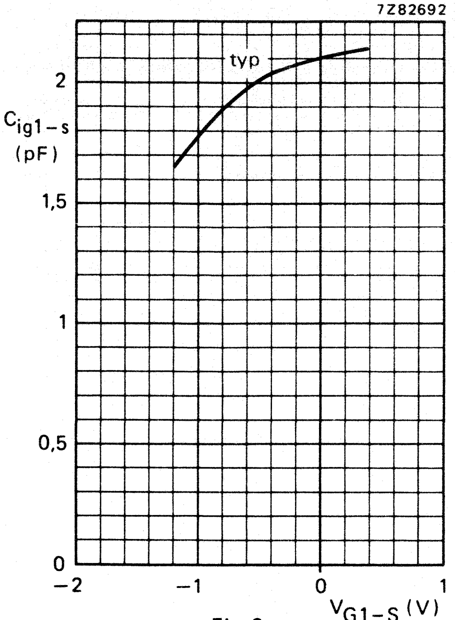


Fig. 6.

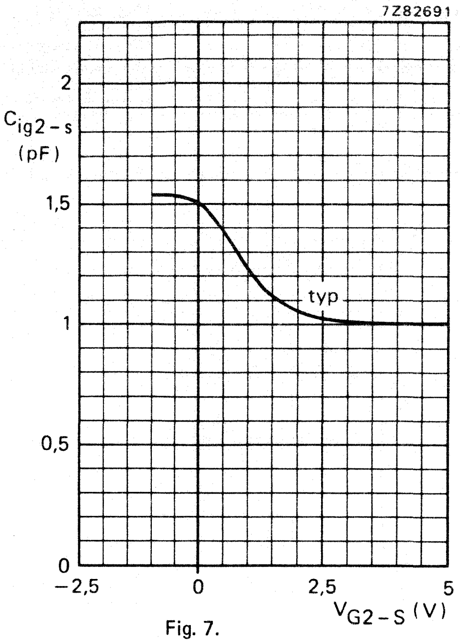


Fig. 7.

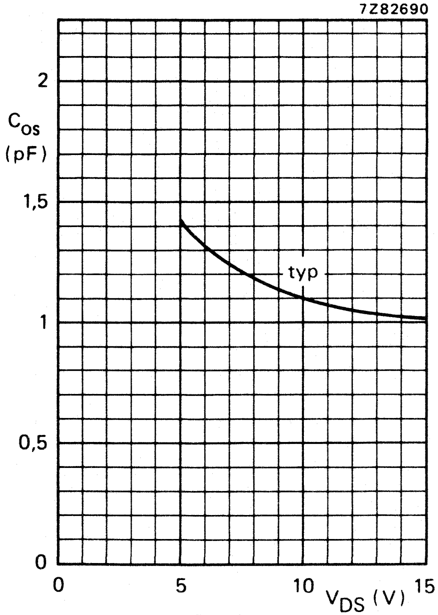


Fig. 8.

Measuring conditions:

Fig. 6 V_{DS} = 10 V; V_{G2-S} = + 4 V; f = 1 MHz; T_{amb} = 25 °C.

Fig. 7 V_{DS} = 10 V; V_{G1-S} = 0; f = 1 MHz; T_{amb} = 25 °C.

Fig. 8 V_{G2-S} = + 4 V; I_D = 10 mA; f = 1 MHz; T_{amb} = 25 °C.

Measuring conditions for Figs 9 to 12: V_{DS} = 10 V; I_D = 10 mA; $V_{G2\text{-}S}$ = + 4 V; T_{amb} = 25 °C.

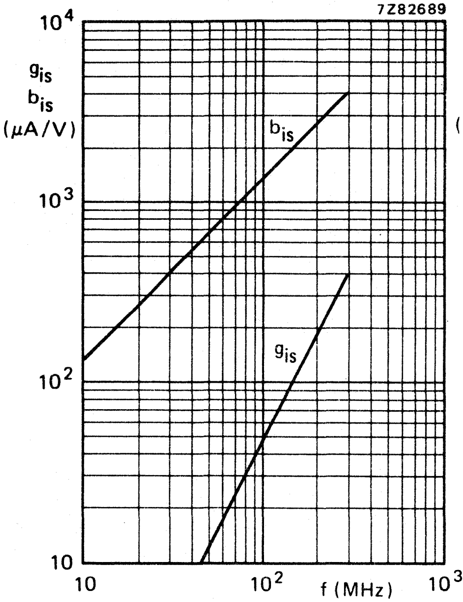


Fig. 9.

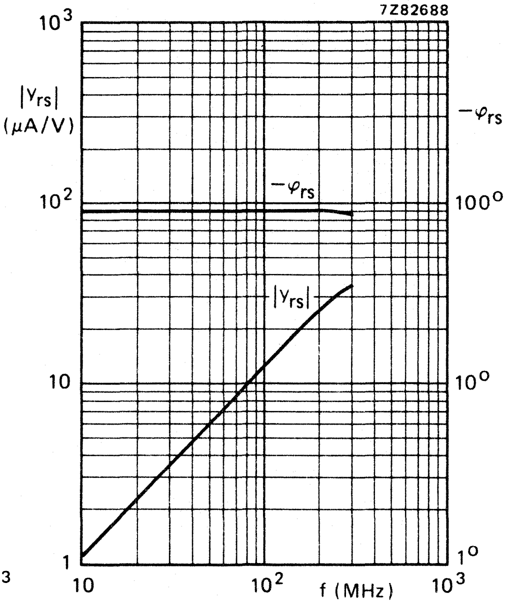


Fig. 10.

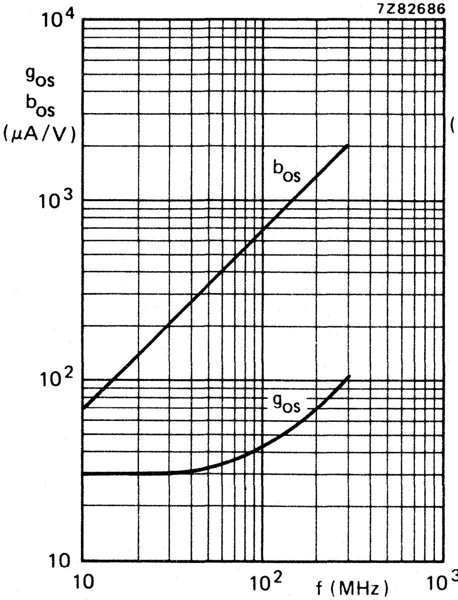


Fig. 11.

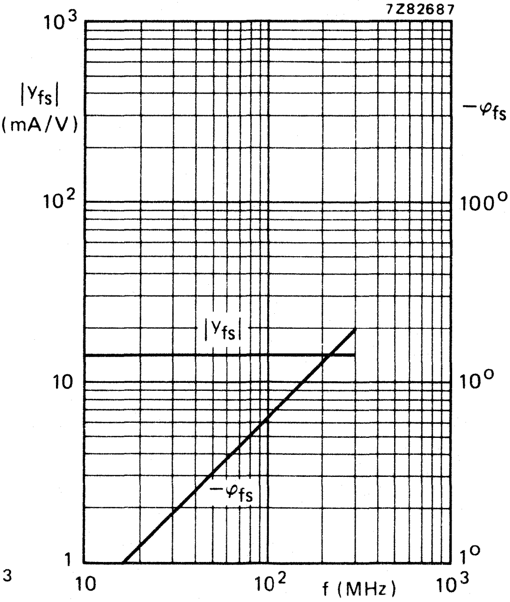


Fig. 12.

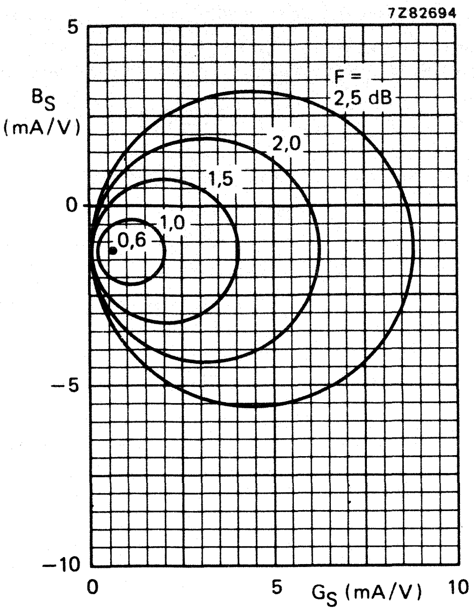


Fig. 13 V_{DS} = 10 V; $V_{G2\text{-}S}$ = + 4 V; I_D = 10 mA; f = 100 MHz; T_{amb} = 25 °C; circles of typical constant noise figures.

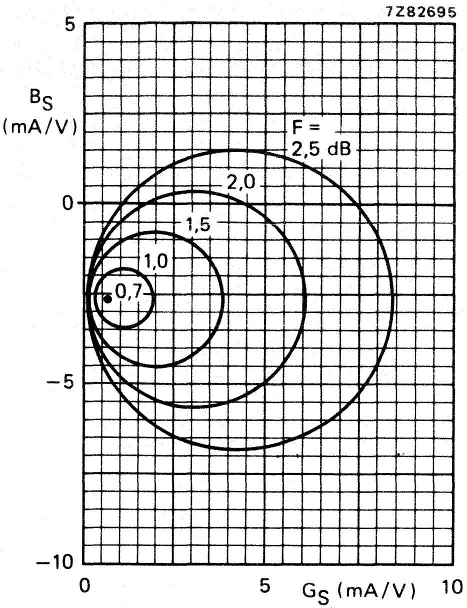
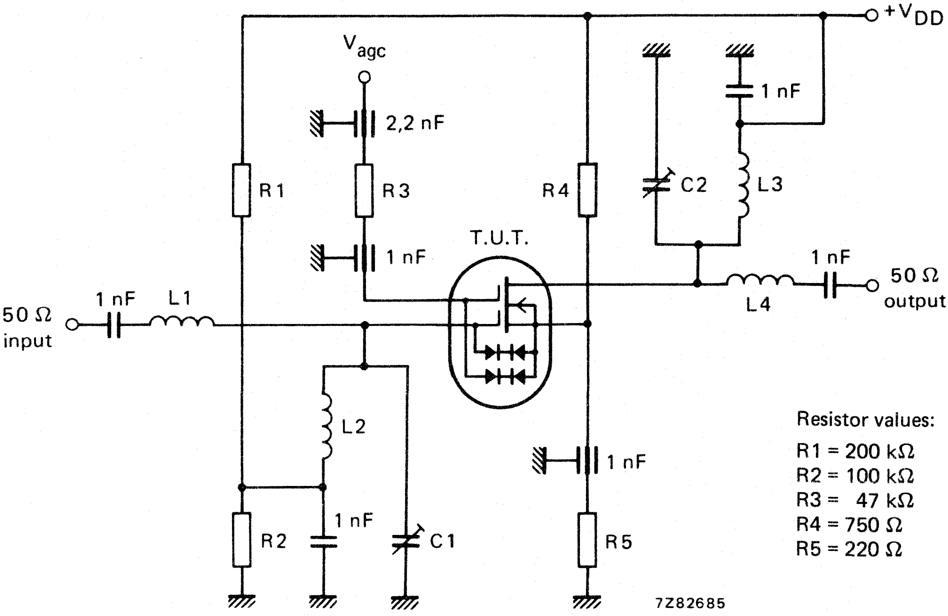


Fig. 14 V_{DS} = 10 V; $V_{G2\text{-}S}$ = + 4 V; I_D = 10 mA; f = 200 MHz; T_{amb} = 25 °C; circles of typical constant noise figures.



Resistor values:
R1 = 200 kΩ
R2 = 100 kΩ
R3 = 47 kΩ
R4 = 750 Ω
R5 = 220 Ω

Fig. 15 Automatic gain control test circuit at f = 200 MHz (see also Fig. 16).
V_{DD} = 16 V; G_S = 2 mA/V; G_L = 0,5 mA/V.

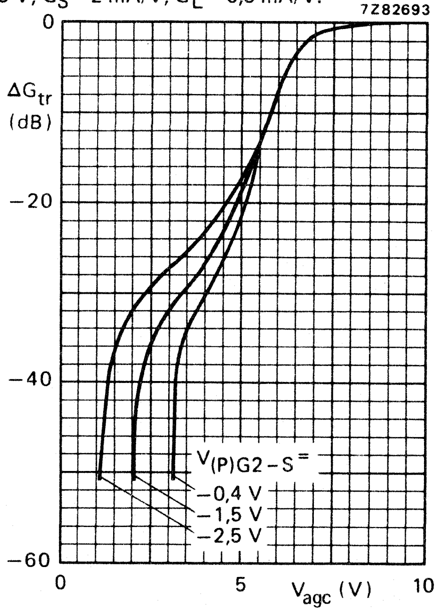


Fig. 16 V_{DD} = 16 V; f = 200 MHz;
T_{amb} = 25 °C; typical values;
see also Fig. 15.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for v.h.f. applications, such as v.h.f. television tuners, f.m. tuners, with 12 V supply voltage.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

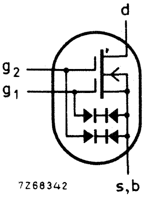
QUICK REFERENCE DATA

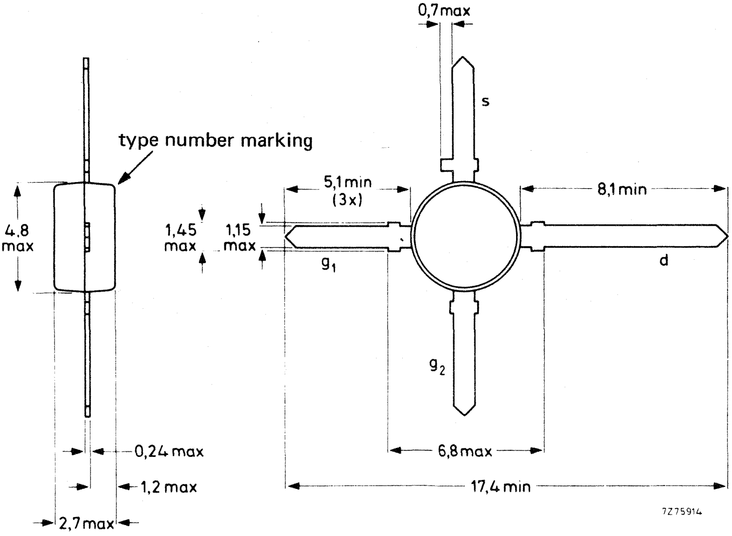
Drain-source voltage	V_{DS}	max.	20	V
Drain current	I_D	max.	40	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225	mW
Junction temperature	T_j	max.	150	°C
Transfer admittance at f = 1 kHz I_D = 15 mA; V_{DS} = 10 V; $+V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs} \rvert$	typ.	25	mA/V
Feedback capacitance at f = 1 MHz I_D = 15 mA; V_{DS} = 10 V; $+V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	30	fF
Noise figure at G_S = 2 mA/V I_D = 15 mA; V_{DS} = 10 V; $+V_{G2\text{-}S}$ = 4 V; f = 200 MHz	F	typ.	1,2	dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-103.





RATINGS

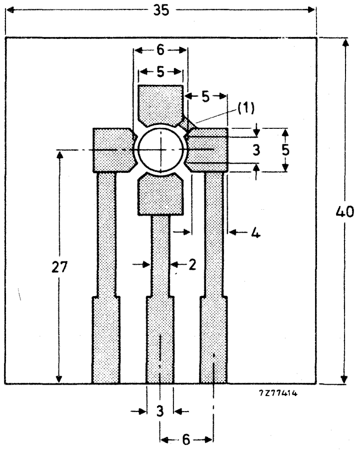
Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain current (d.c. or average)	I_D	max.	40	mA
Gate 1 - source current	$\pm I_{G1\text{-}S}$	max.	10	mA
Gate 2 - source current	$\pm I_{G2\text{-}S}$	max.	10	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225	mW
Storage temperature	T_{stg}	−65 to +	150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air mounted on the printed-circuit board (see Fig. 2)	$R_{th\,j\text{-}a}$	=	335 K/W

Dimensions in mm



(1) Connection made by a strip or Cu wire.

Fig. 2 Single-sided 35 μm Cu-clad epoxy fibre-glass printed-circuit board, thickness 1,5 mm. Tracks are fully tin-lead plated. Board in horizontal position for R_{th} measurement.

STATIC CHARACTERISTICS

T_{amb} = 25 °C

Gate cut-off currents			
$\pm V_{G1-S}$ = 7 V; $V_{G2-S} = V_{DS}$ = 0	$\pm I_{G1-SS}$	<	25 nA
$\pm V_{G2-S}$ = 7 V; $V_{G1-S} = V_{DS}$ = 0	$\pm I_{G2-SS}$	<	25 nA
Gate-source breakdown voltages			
$\pm I_{G1-SS}$ = 10 mA; $V_{G2-S} = V_{DS}$ = 0	$\pm V_{(BR)G1-SS}$	>	8 V
$\pm I_{G2-SS}$ = 10 mA; $V_{G1-S} = V_{DS}$ = 0	$\pm V_{(BR)G2-SS}$	>	8 V
Gate-source cut-off voltages			
I_D = 20 μA; V_{DS} = 10 V; $+V_{G2-S}$ = 4 V	$-V_{(P)G1-S}$	<	1,3 V
I_D = 20 μA; V_{DS} = 10 V; V_{G1-S} = 0	$-V_{(P)G2-S}$	<	1,1 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 15 mA; V_{DS} = 10 V; $+V_{G2-S}$ = 4 V; T_{amb} = 25 °C

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	> typ.	20 mA/V 25 mA/V
Input capacitance at gate 1; f = 1 MHz	C_{ig1-s}	typ.	4,0 pF
Input capacitance at gate 2; f = 1 MHz	C_{ig2-s}	typ.	1,7 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	30 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	2,0 pF
Noise figure at f = 200 MHz; G_S = 2 mA/V	F	typ.	1,2 dB

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT-143 microminiature envelope with source and substrate interconnected. This MOS-FET tetrode is intended for use in u.h.f. applications in television tuners. The device is also suitable for use in professional communication equipment.

The device is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V
Drain current (peak value)	I_{DM}	max.	30	mA
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	max.	200	mW
Junction temperature	T_j	max.	150	°C
Transfer admittance at f = 1 kHz I_D = 7 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$\|y_{fs}\|$	typ.	12	mA/V
Feedback capacitance at f = 1 MHz I_D = 7 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	25	fF
Noise figure at G_S = 2 mA/V I_D = 7 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; f = 800 MHz	F	typ.	2,8	dB

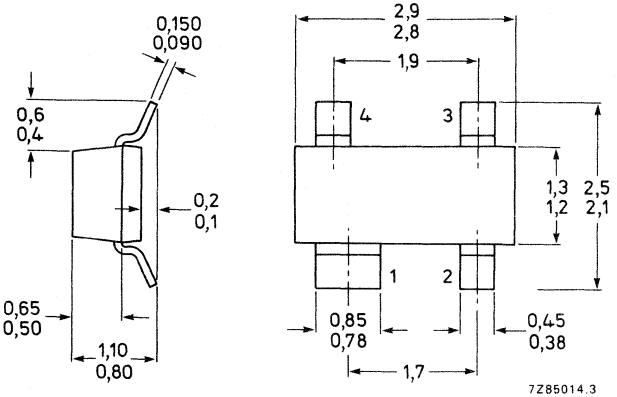
MECHANICAL DATA

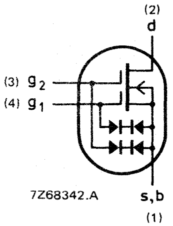
Dimensions in mm

Fig. 1 SOT-143.

Marking code

BF989 = M89





See also *Soldering recommendations*.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20 V
Drain current (d.c. or average)	I_D	max.	20 mA
Drain current (peak value)	I_{DM}	max.	30 mA
Gate 1 - source current	$\pm I_{G1\text{-}S}$	max.	10 mA
Gate 2 - source current	$\pm I_{G2\text{-}S}$	max.	10 mA
Total power dissipation up to $T_{amb} = 60\ ^oC$*	P_{tot}	max.	200 mW
Storage temperature	T_{stg}	−65 to + 150	°C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient in free air*	$R_{th\ j\text{-}a}$	=	460 K/W

STATIC CHARACTERISTICS

$T_{amb} = 25\ ^oC$ unless otherwise specified

Gate cut-off currents			
$\pm V_{G1\text{-}S} = 5$ V; $V_{G2\text{-}S} = V_{DS} = 0$	$\pm I_{G1\text{-}SS}$	<	50 nA
$\pm V_{G2\text{-}S} = 5$ V; $V_{G1\text{-}S} = V_{DS} = 0$	$\pm I_{G2\text{-}SS}$	<	50 nA
Drain current			
$V_{DS} = 10$ V; $V_{G1\text{-}S} = 0$; $+V_{G2\text{-}S} = 4$ V; $T_j = 25\ ^oC$	I_{DSS}		2 to 20 mA
Gate-source breakdown voltages			
$\pm I_{G1\text{-}SS} = 10$ mA; $V_{G2\text{-}S} = V_{DS} = 0$	$\pm V_{(BR)G1\text{-}SS}$		6 to 20 V
$\pm I_{G2\text{-}SS} = 10$ mA; $V_{G1\text{-}S} = V_{DS} = 0$	$\pm V_{(BR)G2\text{-}SS}$		6 to 20 V
Gate-source cut-off voltages			
$I_D = 20\ \mu A$; $V_{DS} = 10$ V; $+V_{G2\text{-}S} = 4$ V	$-V_{(P)G1\text{-}S}$	<	2,7 V
$I_D = 20\ \mu A$; $V_{DS} = 10$ V; $V_{G1\text{-}S} = 0$	$-V_{(P)G2\text{-}S}$	<	2,7 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): $I_D = 7$ mA; $V_{DS} = 10$ V; $+V_{G2\text{-}S} = 4$ V; $T_{amb} = 25\ ^oC$

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	> typ.	9,5 mA/V 12 mA/V
Input capacitance at gate 1; f = 1 MHz	$C_{ig1\text{-}s}$	typ.	1,8 pF
Input capacitance at gate 2; f = 1 MHz	$C_{ig2\text{-}s}$	typ.	1,0 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	0,9 pF
Noise figure at $G_S = 2$ mA/V			
f = 200 MHz	F	typ.	1,6 dB
f = 800 MHz	F	typ.	2,8 dB

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* Device mounted on a ceramic substrate of 8 mm x 10 mm x 0,6 mm.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic microminiature envelope with source and substrate interconnected, intended for u.h.f. applications, such as u.h.f. television tuners and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	18	V
Drain current (average)	$I_{D(AV)}$	max.	30	mA
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	max.	200	mW
Junction temperature	T_j	max.	150	°C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$\|y_{fs}\|$	typ.	21	mA/V
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	25	fF
Noise figure at optimum source admittance I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; f = 800 MHz	F	typ.	2,8	dB

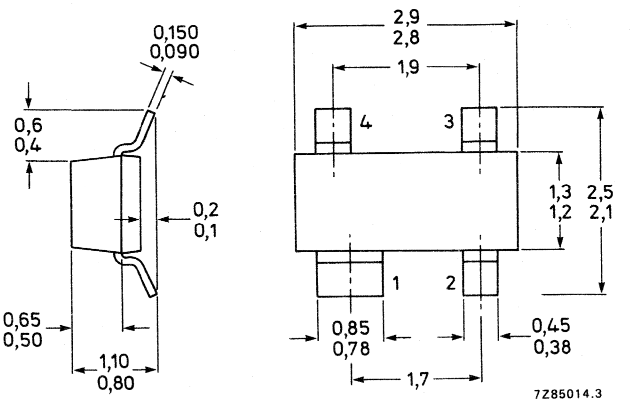
MECHANICAL DATA

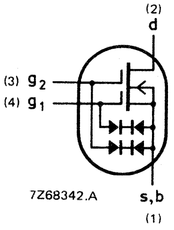
Dimensions in mm

Fig. 1 SOT-143.

Marking code

BF990 = M90





See also *Soldering recommendations.*

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	18	V
Drain current (average)	$I_{D(AV)}$	max.	30	mA
Gate 1 source current	$\pm I_{G1\text{-}S}$	max.	10	mA
Gate 2 source current	$\pm I_{G2\text{-}S}$	max.	10	mA
Total power dissipation up to T_{amb} = 60 °C*	P_{tot}	max.	200	mW
Storage temperature	T_{stg}	−65 to + 150		°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air*	$R_{th\,j\text{-}a}$	=	460	K/W

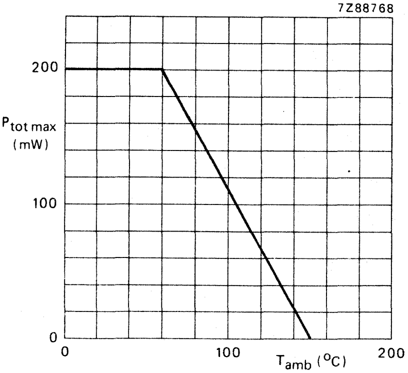


Fig. 2 Power derating curve.

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* Device mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

STATIC CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

Gate cut-off currents				
gate 1; $\pm V_{G1\text{-}S} = 7$ V; $V_{G2\text{-}S} = V_{DS} = 0$	$\pm I_{G1\text{-}SS}$	$<$	25	nA
gate 2; $\pm V_{G2\text{-}S} = 7$ V; $V_{G1\text{-}S} = V_{DS} = 0$	$\pm I_{G2\text{-}SS}$	$<$	25	nA
Gate-source breakdown voltages				
gate 1; $\pm I_{G1\text{-}SS} = 10$ mA; $V_{G2\text{-}S} = V_{DS} = 0$	$\pm V_{(BR)G1\text{-}SS}$	$>$	8	V
gate 2; $\pm I_{G2\text{-}SS} = 10$ mA; $V_{G1\text{-}S} = V_{DS} = 0$	$\pm V_{(BR)G2\text{-}SS}$	$>$	8	V
Gate-source cut-off voltages				
gate 1; $I_D = 20\ \mu$A; $V_{DS} = 10$ V; $+V_{G2\text{-}S} = 4$ V	$-V_{(P)G1\text{-}S}$	$<$	1,3	V
gate 2; $I_D = 20\ \mu$A; $V_{DS} = 10$ V; $V_{G1\text{-}S} = 0$	$-V_{(P)G2\text{-}S}$	$<$	1,1	V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): $I_D = 10$ mA; $V_{DS} = 10$ V; $+V_{G2\text{-}S} = 4$ V; $T_{amb} = 25$ °C

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	$>$ typ.	17 21	mA/V mA/V
Input capacitance at gate 1; f = 1 MHz	$C_{ig1\text{-}s}$	typ.	3	pF
Input capacitance at gate 2; f = 1 MHz	$C_{ig2\text{-}s}$	typ.	1,4	pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25	fF
Output capacitance at f = 1 MHz	C_{os}	typ.	1,2	pF
Noise figure at f = 800 MHz; $G_S = 5$ mA/V	F	typ.	2,8	dB

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT-143 microminiature envelope with source and substrate interconnected. This MOS-FET tetrode is intended for use in v.h.f. applications, such as v.h.f. television tuners and f.m. tuners. The device is also suitable for use in professional communication equipment.

The device is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V
Drain current	I_D	max.	20	mA
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	max.	200	mW
Junction temperature	T_j	max.	150	°C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs} \rvert$	typ.	14	mA/V
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	20	fF
Noise figure at optimum source admittance I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; f = 200 MHz	F	typ.	0,7	dB

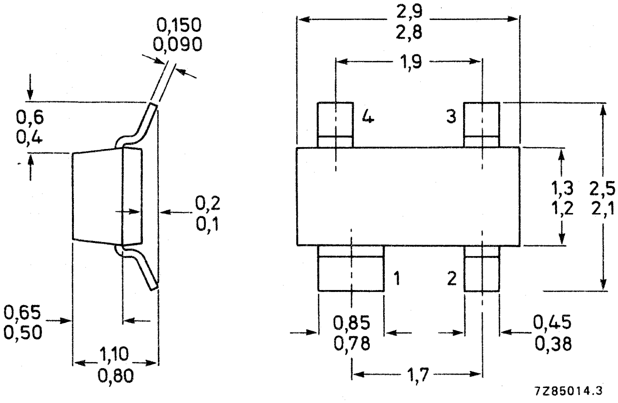
MECHANICAL DATA

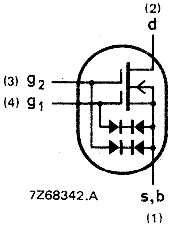
Dimensions in mm

Marking code

BF991 = M91

Fig. 1 SOT-143.





See also *Soldering recommendations.*

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain current (d.c. or average)	I_D	max.	20	mA
Drain current (peak value)	I_{DM}	max.	30	mA
Gate 1 - source current	$\pm I_{G1\text{-}S}$	max.	10	mA
Gate 2 - source current	$\pm I_{G2\text{-}S}$	max.	10	mA
Total power dissipation up to $T_{amb} = 60\ ^{o}C$*	P_{tot}	max.	200	mW
Storage temperature	T_{stg}	−65 to + 150		^{o}C
Junction temperature	T_j	max.	150	^{o}C

THERMAL RESISTANCE

From junction to ambient in free air*	$R_{th\ j\text{-}a}$	=	460	K/W

STATIC CHARACTERISTICS

$T_{amb} = 25\ ^{o}C$ unless otherwise specified

Gate cut-off currents				
$\pm V_{G1\text{-}S} = 5$ V; $V_{G2\text{-}S} = V_{DS} = 0$	$\pm I_{G1\text{-}SS}$	$<$	50	nA
$\pm V_{G2\text{-}S} = 5$ V; $V_{G1\text{-}S} = V_{DS} = 0$	$\pm I_{G2\text{-}SS}$	$<$	50	nA
Drain current				
$V_{DS} = 10$ V; $V_{G1\text{-}S} = 0$; $+V_{G2\text{-}S} = 4$ V; $T_j = 25\ ^{o}C$	I_{DSS}		4 to 25	mA
Gate-source breakdown voltages				
$\pm I_{G1\text{-}SS} = 10$ mA; $V_{G2\text{-}S} = V_{DS} = 0$	$\pm V_{(BR)G1\text{-}SS}$	$>$	6	V
$\pm I_{G2\text{-}SS} = 10$ mA; $V_{G1\text{-}S} = V_{DS} = 0$	$\pm V_{(BR)G2\text{-}SS}$	$>$	6	V
Gate-source cut-off voltages				
$I_D = 20\ \mu A$; $V_{DS} = 10$ V; $+V_{G2\text{-}S} = 4$ V	$-V_{(P)G1\text{-}S}$	$<$	2,5	V
$I_D = 20\ \mu A$; $V_{DS} = 10$ V; $V_{G1\text{-}S} = 0$	$-V_{(P)G2\text{-}S}$	$<$	2,5	V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): $I_D = 10$ mA; $V_{DS} = 10$ V; $+V_{G2\text{-}S} = 4$ V; $T_{amb} = 25\ ^{o}C$

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	$>$ typ.	10 14	mA/V mA/V
Input capacitance at gate 1; f = 1 MHz	$C_{ig1\text{-}s}$	typ.	2,1	pF
Input capacitance at gate 2; f = 1 MHz	$C_{ig2\text{-}s}$	typ.	1,0	pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	20	fF
Output capacitance at f = 1 MHz	C_{os}	typ.	1,1	pF
Noise figure				
f = 100 MHz; $G_S = 1$ mA/V	F	typ. $<$	0,7 1,7	dB dB
f = 200 MHz; $G_S = 2$ mA/V	F	typ. $<$	1,0 2,0	dB dB
Transducer gain **				
f = 100 MHz; $G_S = 1$ mA/V; $G_L = 0{,}5$ mA/V	G_{tr}	typ.	29	dB
f = 200 MHz; $G_S = 2$ mA/V; $G_L = 0{,}5$ mA/V	G_{tr}	typ.	26	dB

* Device mounted on a ceramic substrate of 8 mm x 10 mm x 0,6 mm.

** Crystal mounted in a SOT-103 envelope.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT-143 microminiature envelope with source and substrate interconnected. This MOS-FET tetrode is intended for use in v.h.f. applications, such as v.h.f. television tuners, FM tuners with a 12 volt supply voltage. The device is also suitable for use in professional communication equipment.

The device is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V
Drain current	I_D	max.	40	mA
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	max.	200	mW
Junction temperature	T_j	max.	150	°C
Transfer admittance at f = 1 kHz I_D = 15 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs} \rvert$	typ.	25	mA/V
Feedback capacitance at f = 1 MHz I_D = 15 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	30	fF
Noise figure at G_S = 2 mA/V I_D = 15 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; f = 200 MHz	F	typ.	1,2	dB

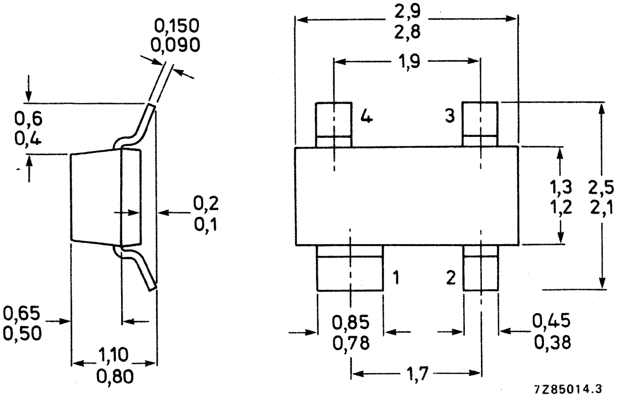
MECHANICAL DATA

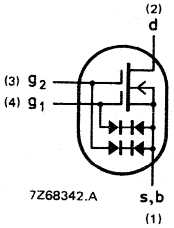
Dimensions in mm

Marking code

BF992 = M92

Fig. 1 SOT-143.





See also *Soldering recommendations*.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20 V
Drain current (d.c. or average)	I_D	max.	40 mA
Gate 1 - source current	$\pm I_{G1\text{-}S}$	max.	10 mA
Gate 2 - source current	$\pm I_{G2\text{-}S}$	max.	10 mA
Total power dissipation up to $T_{amb} = 60\ ^{o}C$*	P_{tot}	max.	200 mW
Storage temperature	T_{stg}	−65 to + 150 °C	
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient in free air*	$R_{th\ j\text{-}a}$	=	460 K/W

STATIC CHARACTERISTICS

$T_{amb} = 25\ ^{o}C$ unless otherwise specified

Gate cut-off currents			
$\pm V_{G1\text{-}S} = 7\ V;\ V_{G2\text{-}S} = V_{DS} = 0$	$\pm I_{G1\text{-}SS}$	$<$	25 nA
$\pm V_{G2\text{-}S} = 7\ V;\ V_{G1\text{-}S} = V_{DS} = 0$	$\pm I_{G2\text{-}SS}$	$<$	25 nA
Gate-source breakdown voltages			
$\pm I_{G1\text{-}SS} = 10\ mA;\ V_{G2\text{-}S} = V_{DS} = 0$	$\pm V_{(BR)G1\text{-}SS}$	$>$	8 V
$\pm I_{G2\text{-}SS} = 10\ mA;\ V_{G1\text{-}S} = V_{DS} = 0$	$\pm V_{(BR)G2\text{-}SS}$	$>$	8 V
Gate-source cut-off voltages			
$I_D = 20\ \mu A;\ V_{DS} = 10\ V;\ +V_{G2\text{-}S} = 4\ V$	$-V_{(P)G1\text{-}S}$		0,2 to 1,3 V
$I_D = 20\ \mu A;\ V_{DS} = 10\ V;\ V_{G1\text{-}S} = 0$	$-V_{(P)G2\text{-}S}$		0,2 to 1,1 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): $I_D = 15\ mA;\ V_{DS} = 10\ V;\ +V_{G2\text{-}S} = 4\ V;\ T_{amb} = 25\ ^{o}C$

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	$>$ typ.	20 mA/V 25 mA/V
Input capacitance at gate 1; f = 1 MHz	$C_{ig1\text{-}s}$	typ.	4 pF
Input capacitance at gate 2; f = 1 MHz	$C_{ig2\text{-}s}$	typ.	1,7 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ. $<$	30 fF 40 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	2 pF
Noise figure at f = 200 MHz; $G_S = 2\ mA/V$	F	typ.	1,2 dB

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* Device mounted on a ceramic substrate of 8 mm x 10 mm x 0,6 mm.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic microminiature envelope with source and substrate interconnected, intended for u.h.f. and v.h.f. applications, such as u.h.f./v.h.f. television tuners and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

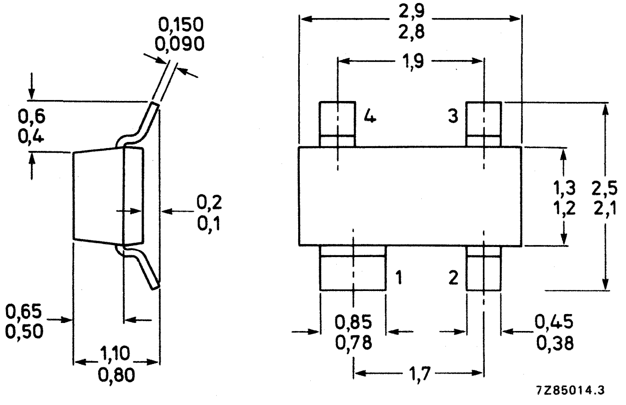
Drain-source voltage	V_{DS}	max.	20	V
Drain current (average)	$I_{D(AV)}$	max.	30	mA
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	max.	200	mW
Junction temperature	T_j	max.	150	°C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$\|y_{fs}\|$	typ.	17	mA/V
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	25	fF
Noise figure at optimum source admittance I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V; f = 200 MHz	F	typ.	1,5	dB

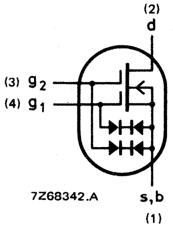
MECHANICAL DATA Dimensions in mm

Fig. 1 SOT-143.

Marking code

BF994 = M94





See also *Soldering recommendations.*

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain current (average)	$I_{D(AV)}$	max.	30	mA
Gate 1 source current	$\pm I_{G1\text{-}S}$	max.	10	mA
Gate 2 source current	$\pm I_{G2\text{-}S}$	max.	10	mA
Total power dissipation up to T_{amb} = 60 °C*	P_{tot}	max.	200	mW
Storage temperature	T_{stg}	−65 to +	150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air*	$R_{th\,j\text{-}a}$	=	460	K/W

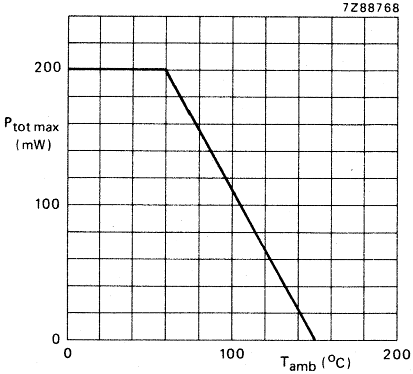


Fig. 2 Power derating curve.

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* Device mounted on a ceramic substrate of 8 mm x 10 mm x 0,6 mm.

STATIC CHARACTERISTICS

$T_{amb} = 25\ ^{o}C$ unless otherwise specified

Gate cut-off currents			
gate 1; $\pm V_{G1\text{-}S} = 5$ V; $V_{G2\text{-}S} = V_{DS} = 0$	$\pm I_{G1\text{-}SS}$	$<$	50 nA
gate 2; $\pm V_{G2\text{-}S} = 5$ V; $V_{G1\text{-}S} = V_{DS} = 0$	$\pm I_{G2\text{-}SS}$	$<$	50 nA
Gate-source breakdown voltages			
gate 1; $\pm I_{G1\text{-}SS} = 10$ mA; $V_{G2\text{-}S} = V_{DS} = 0$	$\pm V_{(BR)G1\text{-}SS}$		6 to 20 V
gate 2; $\pm I_{G2\text{-}SS} = 10$ mA; $V_{G1\text{-}S} = V_{DS} = 0$	$\pm V_{(BR)G2\text{-}SS}$		6 to 20 V
Gate-source cut-off voltages			
gate 1; $I_D = 20\ \mu A$; $V_{DS} = 15$ V; $+V_{G2\text{-}S} = 4$ V	$-V_{(P)G1\text{-}S}$	$<$	2,5 V
gate 2; $I_D = 20\ \mu A$; $V_{DS} = 15$ V; $V_{G1\text{-}S} = 0$	$-V_{(P)G2\text{-}S}$	$<$	2,0 V
Drain-source cut-off voltage $V_{DS} = 15$ V; $V_{G2\text{-}S} = 4$ V	I_{DSS}		2 to 20 mA

DYNAMIC CHARACTERISTCS

Measuring conditions (common source): $I_D = 10$ mA; $V_{DS} = 15$ V; $+V_{G2\text{-}S} = 4$ V; $T_{amb} = 25\ ^{o}C$

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	$>$	15 mA/V
		typ.	17 mA/V
Input capacitance at gate 1; f = 1 MHz	$C_{ig1\text{-}s}$	typ.	2,5 pF
Input capacitance at gate 2; f = 1 MHz	$C_{ig2\text{-}s}$	typ.	1,2 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	1,0 pF
Noise figure at f = 200 MHz; $G_S = 2$ mA/V	F	typ.	1,5 dB
		$<$	2,8 dB
Power gain at $G_S = 2$ mA/V $G_L = 0{,}5$ mA/V, f = 200 MHz	G_p	typ.	25 dB

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic microminiature envelope, with source and substrate interconnected, intended for u.h.f. applications, such as television tuners and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V
Drain current (average)	$I_{D(AV)}$	max.	30	mA
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	max.	200	mW
Junction temperature	T_j	max.	150	°C
Transfer admittance at f = 1 kHz				
I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs} \rvert$	typ.	17	mA/V
Feedback capacitance at f = 1 MHz				
I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	25	fF
Noise figure at optimum source admittance				
I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; f = 800 MHz	F	typ.	2,8	dB
I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V; f = 200 MHz	F	typ.	1,5	dB

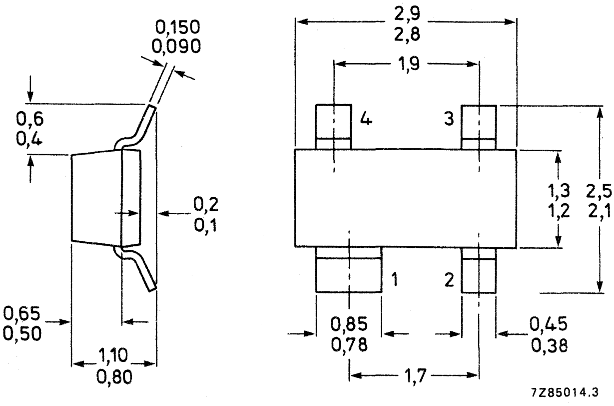
MECHANICAL DATA

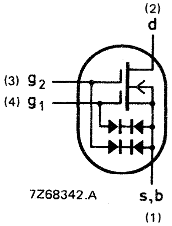
Dimensions in mm

Fig. 1 SOT-143.

Marking code

BF996 = M96





See also *Soldering recommendations.*

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain current (average)	$I_{D(AV)}$	max.	30	mA
Gate 1 source current	$\pm I_{G1\text{-}S}$	max.	10	mA
Gate 2 source current	$\pm I_{G2\text{-}S}$	max.	10	mA
Total power dissipation up to T_{amb} = 60 °C*	P_{tot}	max.	200	mW
Storage temperature	T_{stg}	–65 to + 150		°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air*	$R_{th\,j\text{-}a}$	=	460	K/W

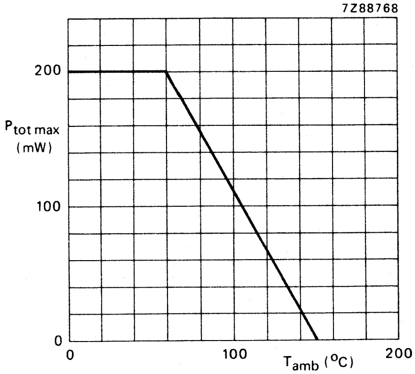


Fig. 2 Power derating curve.

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* Device mounted on a ceramic substrate of 8 mm x 10 mm x 0,6 mm.

STATIC CHARACTERISTICS

$T_{amb} = 25\ ^{o}C$ unless otherwise specified

Gate cut-off currents				
gate 1; $\pm V_{G1\text{-}S} = 5$ V; $V_{G2\text{-}S} = V_{DS} = 0$	$\pm I_{G1\text{-}SS}$	$<$	50	nA
gate 2; $\pm V_{G2\text{-}S} = 5$ V; $V_{G1\text{-}S} = V_{DS} = 0$	$\pm I_{G2\text{-}SS}$	$<$	50	nA
Gate-source breakdown voltages				
gate 1; $\pm I_{G1\text{-}SS} = 10$ mA; $V_{G2\text{-}S} = V_{DS} = 0$	$\pm V_{(BR)G1\text{-}SS}$		6 to 20	V
gate 2; $\pm I_{G2\text{-}SS} = 10$ mA; $V_{G1\text{-}S} = V_{DS} = 0$	$\pm V_{(BR)G2\text{-}SS}$		6 to 20	V
Gate-source cut-off voltages				
gate 1; $I_D = 20\ \mu A$; $V_{DS} = 15$ V; $+V_{G2\text{-}S} = 4$ V	$-V_{(P)G1\text{-}S}$	$<$	2,5	V
gate 2; $I_D = 20\ \mu A$; $V_{DS} = 15$ V; $V_{G1\text{-}S} = 0$	$-V_{(P)G2\text{-}S}$	$<$	2,0	V
Drain-source cut-off voltage $V_{DS} = 15$ V; $V_{G2\text{-}S} = 4$ V	I_{DSS}		2 to 20	mA

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): $I_D = 10$ mA; $V_{DS} = 15$ V; $+V_{G2\text{-}S} = 4$ V; $T_{amb} = 25\ ^{o}C$

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	$>$	15	mA/V
		typ.	17	mA/V
Input capacitance at gate 1; f = 1 MHz	$C_{ig1\text{-}s}$	typ.	2,2	pF
Input capacitance at gate 2; f = 1 MHz	$C_{ig2\text{-}s}$	typ.	1,1	pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25	fF
Output capacitance at f = 1 MHz	C_{os}	typ.	0,8	pF
Noise figure				
at $G_S = 2$ mA/V, f = 200 MHz	F	typ.	1,5	dB
at $G_S = 2$ mA/V, f = 800 MHz	F	typ.	2,8	dB
		$<$	3,9	dB
Power gain				
$G_S = 2$ mA/V, $G_L = 0{,}5$ mA/V, f = 200 MHz	G_p	typ.	25	dB
$G_S = 2$ mA/V, $G_L = 1{,}0$ mA/V, f = 800 MHz	G_p	typ.	18	dB

N-CHANNEL INSULATED GATE MOS-FET

Depletion type field-effect transistor in a TO-72 metal envelope with the substrate connected to the case. It is intended for linear applications in the audio as well as the i.f. and v.h.f. frequency region, and in cases where high input impedance, low gate leakage currents and low noise figures are of importance.

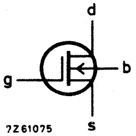
QUICK REFERENCE DATA

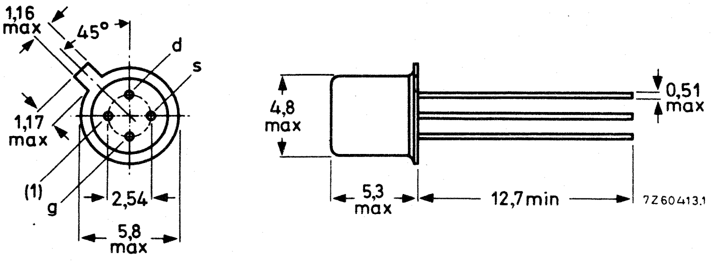
Drain-substrate voltage	V_{DB}	max.	30 V
Gate-substrate voltage (continuous)	$\pm V_{GB}$	max.	10 V
Drain current $V_{DS} = 15$ V; $V_{GS} = 0$	I_{DSS}		10 to 40 mA
Transfer admittance $I_D = 5$ mA; $V_{DS} = 15$ V; f = 1 kHz	$\lvert y_{fs} \rvert$	>	6 mA/V
Feedback capacitance $I_D = 5$ mA; $V_{DS} = 15$ V; f = 1 MHz	C_{rs}	<	0,7 pF
Noise figure at f = 200 MHz $I_D = 5$ mA; $V_{DS} = 15$ V; $T_{amb} = 25$ °C $G_S = 1$ mA/V; $B_S = B_{Sopt}$	F	<	5 dB
Equivalent noise voltage at f = 1 kHz $I_D = 5$ mA; $V_{DS} = 15$ V; $T_{amb} = 25$ °C	$V_n/\sqrt{B}$	typ.	100 nV/$\sqrt{\text{Hz}}$

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-72.





(1) = substrate (b) connected to case

Accessories: 56246 (distance disc).

Note

To safeguard the gates against damage due to accumulation of static charge during transport or handling, the leads are encircled by a ring of conductive rubber which should be removed just after the transistor is soldered into the circuit.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

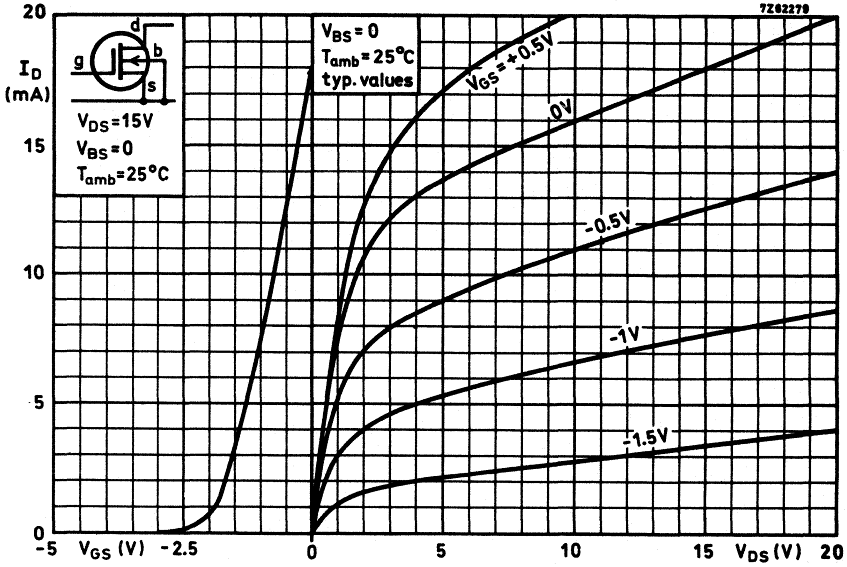
Drain-substrate voltage	V_{DB}	max.	30	V
Source-substrate voltage	V_{SB}	max.	30	V
Gate-substrate voltage (continuous)	$\pm V_{GB}$	max.	10	V
Repetitive peak gate to all other terminals voltage $V_{SB} = V_{DB} = 0$; $f > 100$ Hz	V_{G-N}	max. min.	15 −15	V V
Drain current (d.c.)	I_D	max.	20	mA
Drain current (peak value) $t_p = 20$ ms; $\delta = 0,1$	I_{DM}	max.	50	mA
Total power dissipation up to $T_{amb} = 25$ °C	P_{tot}	max.	200	mW
Storage temperature	T_{stg}	−65 to + 125		°C
Junction temperature	T_j	max.	125	°C

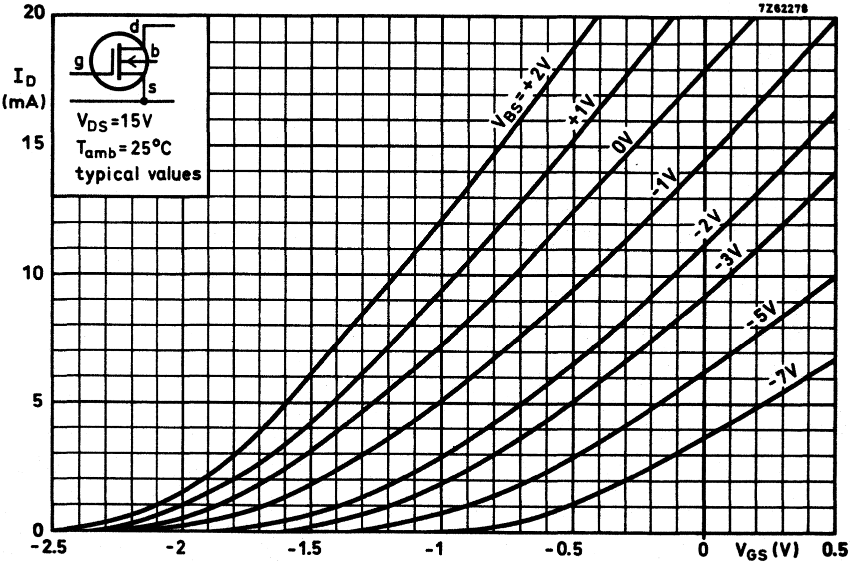
THERMAL RESISTANCE

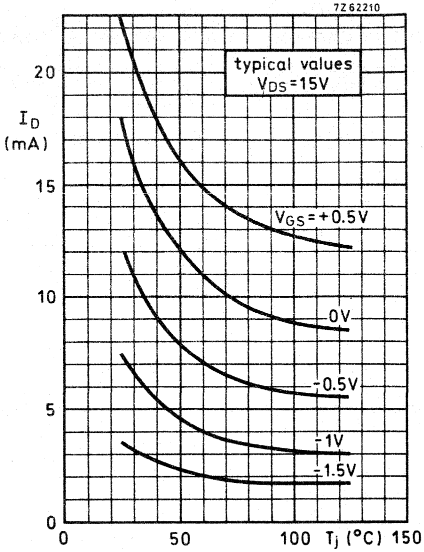
From junction to ambient in free air	$R_{th\,j\text{-}a}$	=	500	K/W

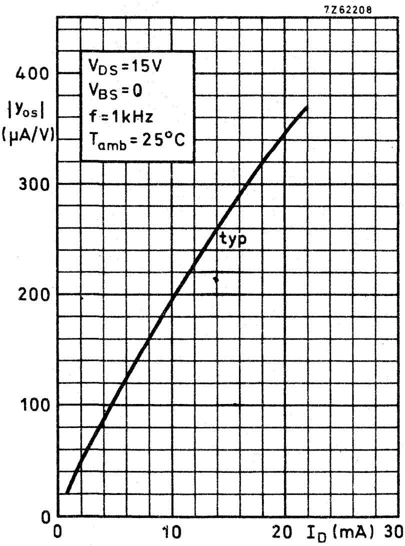
CHARACTERISTICS $T_j = 25\ ^{\circ}C$ unless otherwise specified

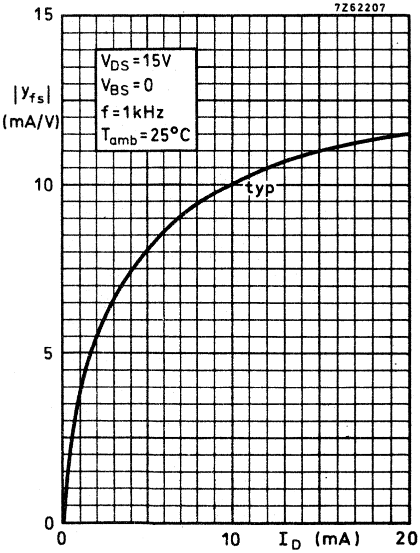
Gate currents; $V_{BS} = 0$				
$-V_{GS} = 10\ V;\ V_{DS} = 0$	$-I_{GSS}$	$<$	10	pA
$V_{GS} = 10\ V;\ V_{DS} = 0$	I_{GSS}	$<$	10	pA
$-V_{GS} = 10\ V;\ V_{DS} = 0;\ T_j = 125\ ^{\circ}C$	$-I_{GSS}$	$<$	200	pA
$V_{GS} = 10\ V;\ V_{DS} = 0;\ T_j = 125\ ^{\circ}C$	I_{GSS}	$<$	200	pA
Bulk currents; $V_{GB} = 0$				
$-V_{BD} = 30\ V;\ I_S = 0$	$-I_{BDO}$	$<$	10	μA
$-V_{BS} = 30\ V;\ I_D = 0$	$-I_{BSO}$	$<$	10	μA
Drain current				
$V_{DS} = 15\ V;\ V_{GS} = 0$	I_{DSS}		10 to 40	mA
Gate-source voltage				
$I_D = 100\ nA;\ V_{DS} = 15\ V$	$-V_{GS}$		0.5 to 3.5	V
Gate-source cut-off voltage				
$I_D = 100\ nA;\ V_{DS} = 15\ V$	$-V_{(P)GS}$	$<$	4	V
y parameters $T_{amb} = 25\ ^{\circ}C$				
$I_D = 5\ mA;\ V_{DS} = 15\ V$				
Transfer admittance at f = 1 kHz	$\lvert y_{fs}\rvert$	$>$	6	mA/V
Output admittance at f = 1 kHz	$\lvert y_{os}\rvert$	$<$	0.4	mA/V
Input capacitance at f = 1 MHz	C_{is}	$<$	5	pF
Feedback capacitance at f = 1 MHz	C_{rs}	$<$	0.7	pF
Output capacitance at f = 1 MHz	C_{os}	$<$	3	pF
Noise figure at f = 200 MHz $T_{amb} = 25\ ^{\circ}C$				
$I_D = 5\ mA;\ V_{DS} = 15\ V$				
$G_S = 1\ m\Omega^{-1};\ B_S = B_{Sopt}$	F	$<$	5	dB
Equivalent noise voltage $T_{amb} = 25\ ^{\circ}C$				
$I_D = 5\ mA;\ V_{DS} = 15\ V;\ f = 120\ Hz$	$V_n/\sqrt{B}$	typ.	300	$nV/\sqrt{Hz}$
$f = 1\ kHz$	$V_n/\sqrt{B}$	typ.	100	$nV/\sqrt{Hz}$
$f = 10\ kHz$	$V_n/\sqrt{B}$	typ.	35	$nV/\sqrt{Hz}$

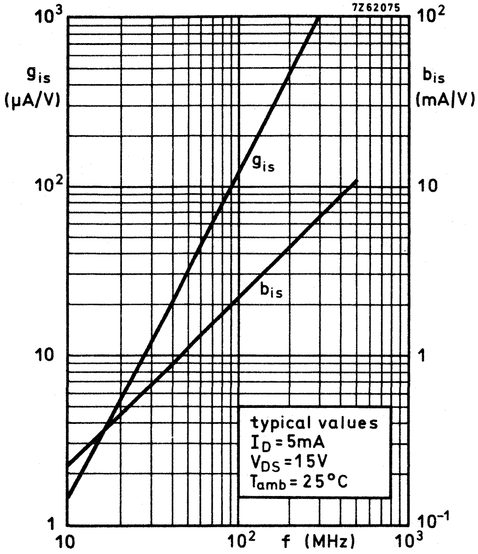

7Z62279
I_D (mA)
20
15
10
5
0
-5
V_GS (V)
-2.5
0
5
10
15
V_DS (V)
20
d
g
b
s
V_DS = 15V
V_BS = 0
T_amb = 25°C
V_BS = 0
T_amb = 25°C
typ. values
V_GS = +0.5V
0V
-0.5V
-1V
-1.5V

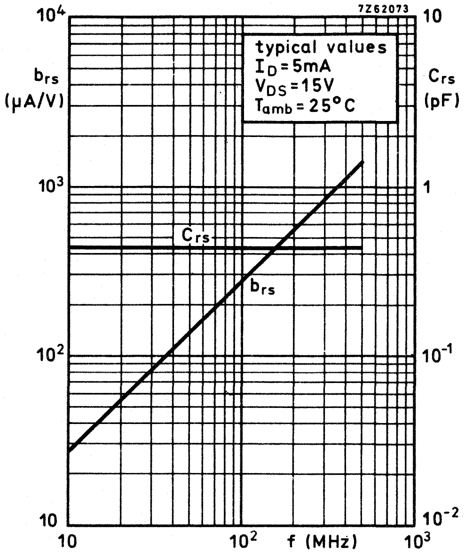

7Z62278
I_D (mA)
20
15
10
5
0
-2.5
-2
-1.5
-1
-0.5
0
V_GS (V)
0.5
d
g
b
s
V_DS = 15V
T_amb = 25°C
typical values
V_BS = +2V
+1V
0V
-1V
-2V
-3V
-5V
-7V

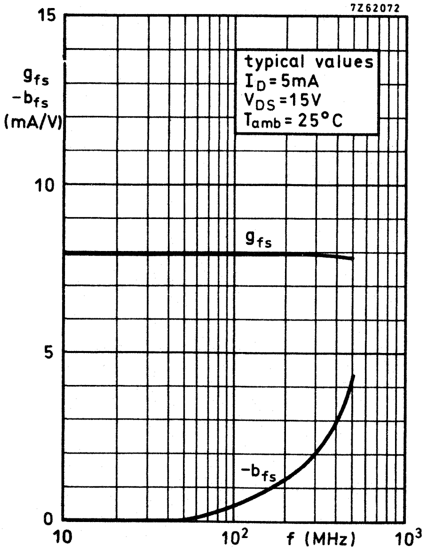

7Z62210
typical values
V_{DS} = 15V
I_D (mA)
0
5
10
15
20
V_{GS} = +0.5V
0V
-0.5V
-1V
-1.5V
0
50
100
T_j (°C)
150

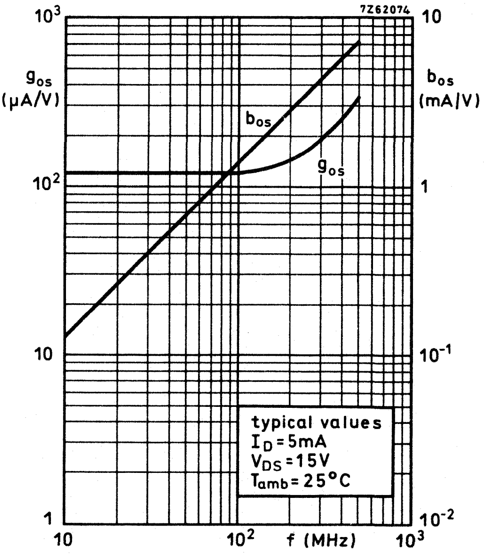

7Z62208
V_{DS} = 15V
V_{BS} = 0
f = 1kHz
T_{amb} = 25°C
$|y_{os}|$ (μA/V)
0
100
200
300
400
typ
0
10
20
I_D (mA)
30

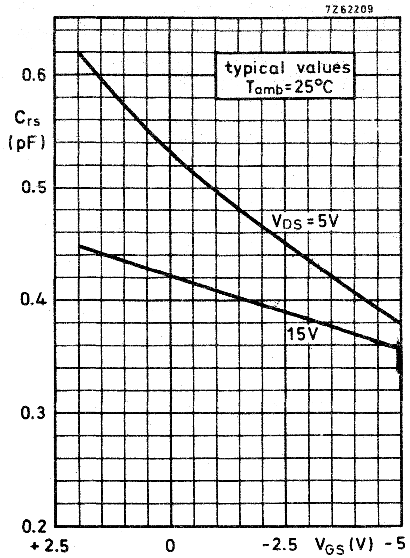

7Z62207
V_{DS} = 15V
V_{BS} = 0
f = 1kHz
T_{amb} = 25°C
$|y_{fs}|$ (mA/V)
0
5
10
15
typ
0
10
I_D (mA)
20

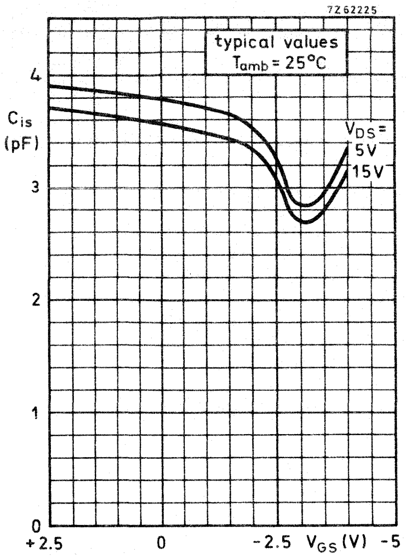

7Z62075
10^3
10^2
10
1
g_is
(μA/V)
10^2
10
1
10^-1
b_is
(mA/V)
g_is
b_is
typical values
I_D = 5mA
V_DS = 15V
T_amb = 25°C
10
10^2
f (MHz)
10^3


7Z62073
10^4
10^3
10^2
10
b_rs
(μA/V)
10
1
10^-1
10^-2
C_rs
(pF)
typical values
I_D = 5mA
V_DS = 15V
T_amb = 25°C
C_rs
b_rs
10
10^2
f (MHz)
10^3


7Z62072
15
10
5
0
g_fs
-b_fs
(mA/V)
typical values
I_D = 5mA
V_DS = 15V
T_amb = 25°C
g_fs
-b_fs
10
10^2
f (MHz)
10^3


7Z62074
10^3
10^2
10
1
g_os
(μA/V)
10
1
10^-1
10^-2
b_os
(mA/V)
b_os
g_os
typical values
I_D = 5mA
V_DS = 15V
T_amb = 25°C
10
10^2
f (MHz)
10^3


7Z62209
typical values
T_{amb} = 25°C
C_{rs}
(pF)
0.6
0.5
0.4
0.3
0.2
V_{DS} = 5V
15V
+2.5
0
-2.5
V_{GS} (V)
-5


7Z62225
typical values
T_{amb} = 25°C
C_{is}
(pF)
4
3
2
1
0
V_{DS} =
5V
15V
+2.5
0
-2.5
V_{GS} (V)
-5

SILICON N-CHANNEL DUAL IG-MOS-FET

Depletion type field-effect transistor in a TO-72 metal envelope with source and substrate connected to the case, intended for a wide range of v.h.f. applications, such as v.h.f. television tuners, f.m. tuners, as well as for applications in communication, instrumentation and control.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

The tetrode configuration, a series arrangement of two gate controlled channels, offers:

a) very low feedback capacitance providing the possibility of more than 40 dB gain control in r.f. amplifiers requiring negligible a.g.c. power.

b) excellent signal handling capability over the entire gain control range.

c) low noise figure combined with high gain.

QUICK REFERENCE DATA

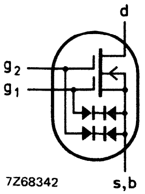
Drain-source voltage	V_{DS}	max.	20	V
Drain current	I_D	max.	50	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300	mW
Junction temperature	T_j	max.	175	°C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V	$\lvert y_{fs} \rvert$	typ.	15	mA/V
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V	C_{rs}	typ.	30	fF
Noise figure at optimum source admittance I_D = 10 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V G_S = 1,2 mA/V; $-B_S$ = 5,7 mA/V; f = 200 MHz	F	typ.	2,3	dB

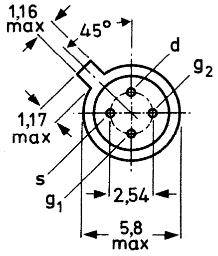
MECHANICAL DATA

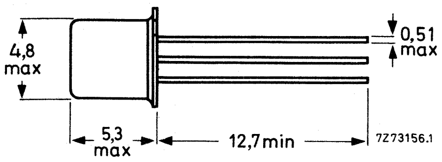
Dimensions in mm

Fig. 1 TO-72.

Source and substrate connected to the case.







Accessories: 56246 (distance disc).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage

Drain-source voltage	V_{DS}	max.	20	V

Currents

Drain current (d.c. or average)	I_D	max.	50	mA
Drain current (peak value)	I_{DM}	max.	100	mA
Gate 1-source current	$\pm I_{G1-S}$	max.	10	mA
Gate 2-source current	$\pm I_{G2-S}$	max.	10	mA

Power dissipation

Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300	mW

Temperatures

Storage temperature	T_{stg}	−65 to + 175		°C
Junction temperature	T_j	max.	175	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j-a}$	=	0,5	°C/mW

STATIC CHARACTERISTICS

$T_{amb} = 25$ °C unless otherwise specified

Gate cut-off currents

$\pm V_{G1-S} = 5$ V; $V_{G2-S} = V_{DS} = 0$	$\pm I_{G1-SS}$	<	10	nA
$\pm V_{G1-S} = 5$ V; $V_{G2-S} = V_{DS} = 0$; $T_j = 150$ °C	$\pm I_{G1-SS}$	<	10	µA
$\pm V_{G2-S} = 5$ V; $V_{G1-S} = V_{DS} = 0$	$\pm I_{G2-SS}$	<	10	nA
$\pm V_{G2-S} = 5$ V; $V_{G1-S} = V_{DS} = 0$; $T_j = 150$ °C	$\pm I_{G2-SS}$	<	10	µA

Gate-source breakdown voltages

$\pm I_{G1-SS} = 0,1$ mA; $V_{G2-S} = V_{DS} = 0$	$\pm V_{(BR)G1-SS}$	6,0 to 20	V
$\pm I_{G2-SS} = 0,1$ mA; $V_{G1-S} = V_{DS} = 0$	$\pm V_{(BR)G2-SS}$	6,0 to 20	V

Drain current

$V_{DS} = 10$ V; $V_{G1-S} = 0$; $+V_{G2-S} = 4$ V	I_{DSS}	20 to 55	mA 1)

Gate 1-source voltage

$I_D = 10$ mA; $V_{DS} = 10$ V; $+V_{G2-S} = 4$ V	$-V_{G1-S}$	0,6 to 2,1	V

Gate-source cut-off voltages

$I_D = 10$ µA ; $V_{DS} = 10$ V; $+V_{G2-S} = 4$ V	$-V_{(P)G1-S}$	1,5 to 3,8	V
$I_D = 10$ µA ; $V_{DS} = 10$ V; $V_{G1-S} = 0$	$-V_{(P)G2-S}$	1,5 to 3,4	V

---

1) Measured under pulse conditions.

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): $I_D = 10$ mA; $V_{DS} = 10$ V; $+V_{G2\text{-}S} = 4$ V; $T_{amb} = 25$ °C

Transfer admittance at f = 1 kHz	$\|y_{fs}\|$	> typ.	12 15	mA/V mA/V
Input capacitance at f = 1 MHz	C_{is}	typ.	5,5	pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	30	fF
Output capacitance at f = 1 MHz	C_{os}	typ.	3,5	pF
Noise figure at optimum source admittance				
$G_S = 0,95$ mA/V; $-B_S = 5,0$ mA/V; f = 100 MHz	F	typ.	1,9	dB
$G_S = 1,20$ mA/V; $-B_S = 5,7$ mA/V; f = 200 MHz	F	typ. <	2,3 3,0	dB dB
Cross modulation at f = 200 MHz				
Wanted signal at f_o = 197,5 MHz Unwanted signal at f_{int} = 202,5 MHz				
Interference voltage at g_1 for K = 1%	V_{int}	typ.	100	mV [1]

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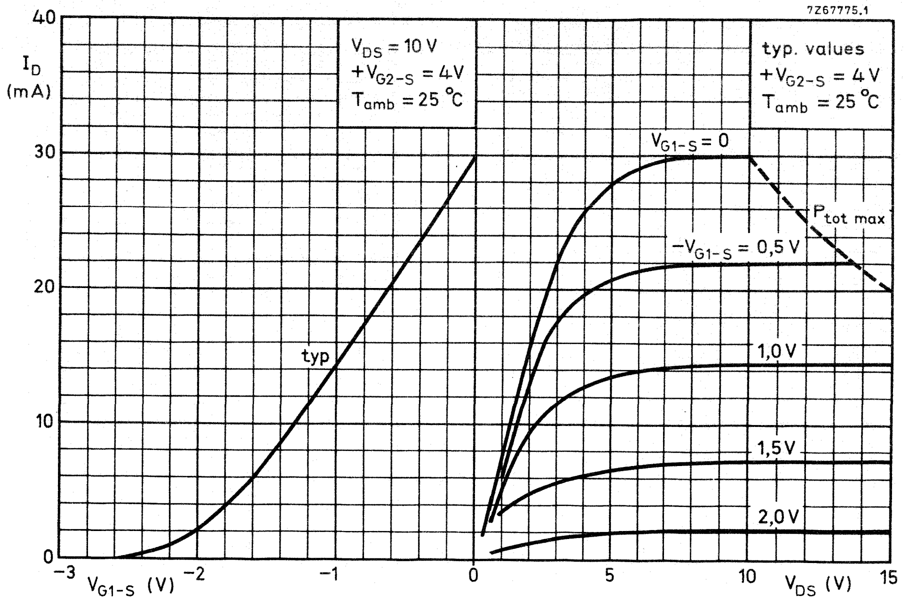
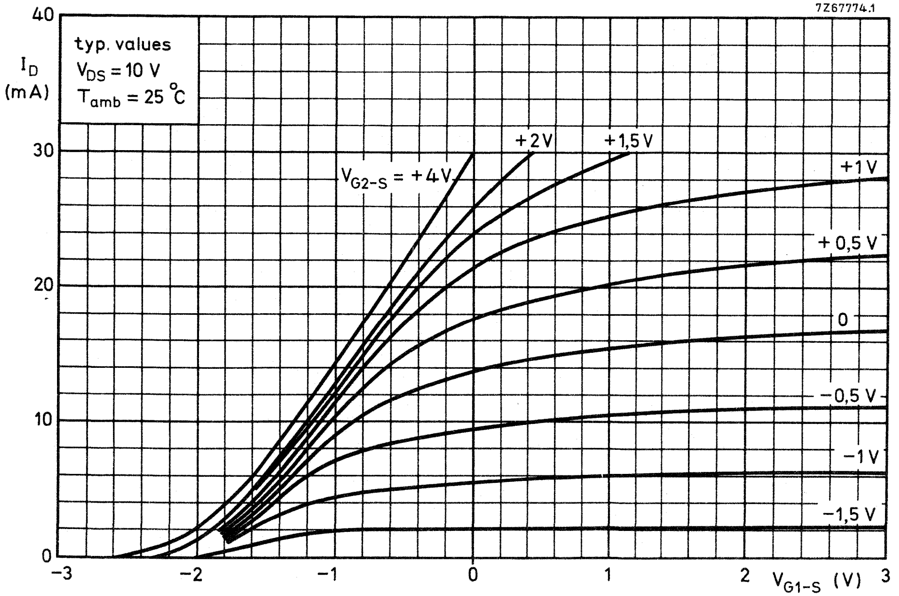
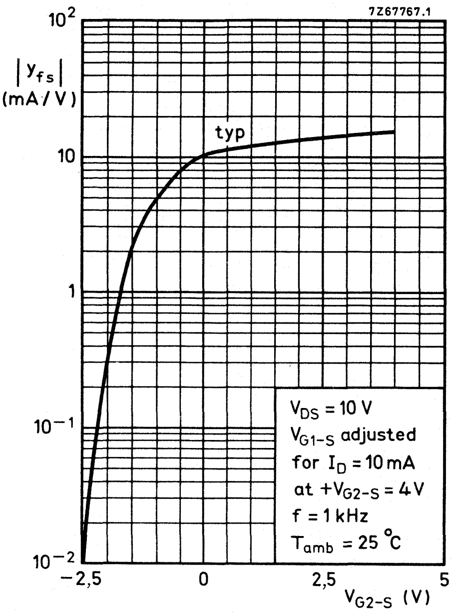
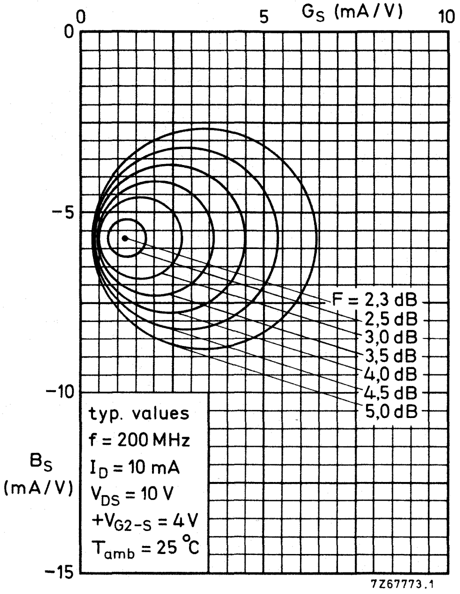
[1] Cross modulation is defined here as the voltage at g_1 of an unwanted signal with 80% modulation depth, giving 0,8% modulation depth on the wanted signal (a.m. definition).


7Z67775.1
40
30
20
10
0
I_D
(mA)
V_DS = 10 V
+V_G2-S = 4 V
T_amb = 25 °C
typ. values
+V_G2-S = 4 V
T_amb = 25 °C
typ
V_G1-S = 0
P_tot max
−V_G1-S = 0,5 V
1,0 V
1,5 V
2,0 V
−3
−2
−1
0
V_G1-S (V)
5
10
15
V_DS (V)


7Z67774.1
40
30
20
10
0
I_D
(mA)
typ. values
V_DS = 10 V
T_amb = 25 °C
V_G2-S = +4 V
+2 V
+1,5 V
+1 V
+0,5 V
0
−0,5 V
−1 V
−1,5 V
−3
−2
−1
0
1
2
3
V_G1-S (V)





circles of constant noise figure

MOSFET N-CHANNEL DEPLETION SWITCHING TRANSISTORS

Symmetrical insulated-gate silicon MOS field-effect transistor of the N-channel depletion mode type.

The transistor is sealed in a TO-72 envelope and features a low ON-resistance and low capacitances.

The transistor is protected against excessive input voltages by integrated back-to-back diodes between gate and substrate.

Applications:

- analog and/or digital switch
- switch driver
- convertor
- chopper

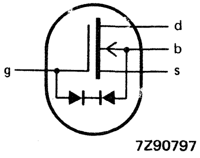
QUICK REFERENCE DATA

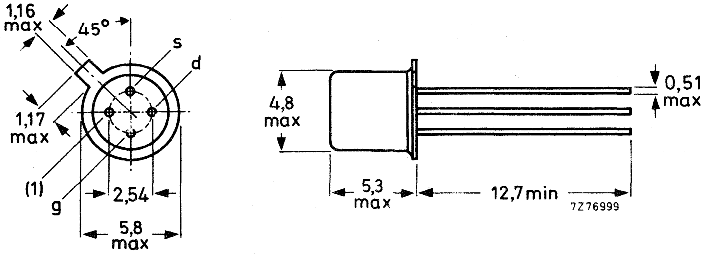
			BSD10	BSD12	
Drain-source voltage	V_{DS}	max.	10	20	V
Gate-source voltage	V_{GS}	max.	+ 10 −30	+ 20 −40	V V
Drain current (d.c.)	I_D	max.	50		mA
Total power dissipation up to T_{amb} = 25 °C (free air)	P_{tot}	max.	275		mW
Junction temperature	T_j	max.	125		°C
Drain-source ON-resistance V_{GS} = 10 V; V_{SB} = 0; I_D = 1 mA	R_{DSon}	<	30		Ω
Feedback capacitance $V_{GS} = V_{BS}$ = −5 V; V_{DS} = 10 V; f = 1 MHz	C_{rss}	typ.	0,6		pF

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-72.





(1) Substrate (b) connected to case.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			BSD10	BSD12	
Drain-source voltage	V_{DS}	max.	10	20	V
Source-drain voltage	V_{SD}	max.	10	20	V
Drain-substrate voltage	V_{DB}	max.	15	25	V
Source-substrate voltage	V_{SB}	max.	15	25	V
Gate-substrate voltage	V_{GB}	max.	+15 −15	+15 −15	V V
Gate-source voltage	V_{GS}	max.	+15 −30	+15 −40	V V
Drain current (d.c.)	I_D	max.	50		mA
Total power dissipation up to T_{amb} = 25 °C in free air	P_{tot}	max.	275		mW
Storage temperature	T_{stg}		−65 to +150		°C
Junction temperature	T_j	max.	125		°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	360	K/W

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

			BSD10	BSD12	
Drain-source breakdown voltage $V_{GS} = V_{BS} = -5$ V; $I_S = 10$ nA	$V_{(BR)DSX}$	>	10	20	V
Source-drain breakdown voltage $V_{GD} = V_{BD} = -5$ V; $I_D = 10$ nA	$V_{(BR)SDX}$	>	10	20	V
Drain-substrate breakdown voltage $V_{GB} = 0$; $I_D = 10$ nA; open source	$V_{(BR)DBO}$	>	15	25	V
Source-substrate breakdown voltage $V_{GB} = 0$; $I_S = 10$ nA; open drain	$V_{(BR)SBO}$	>	15	25	V
Drain-source leakage current $V_{GS} = V_{BS} = -5$ V; $V_{DS} = 10$ V	I_{DSoff}	typ.	1,0		nA
Source-drain leakage current $V_{GD} = V_{BD} = -5$ V; $V_{SD} = 10$ V	I_{SDoff}	typ.	1,0		nA
Gate-substrate leakage current $V_{DB} = V_{SB} = 0$; $V_{GB} = \pm 15$ V	I_{GSoff}	<	10		nA
Forward transconductance at f = 1 kHz $V_{DS} = 10$ V; $V_{SB} = 0$; $I_S = 20$ mA	g_{fs}	> typ.	10 15		mS mS

Gate-source cut-off voltage $V_{DS} = 10$ V; $V_{SB} = 0$; $I_S = 10\ \mu A$	$-V_{(P)GS}$	<	2,0 V
Drain-source ON-resistance $I_D = 1$ mA; $V_{SB} = 0$ $V_{GS} = 5$ V	r_{DSon}	typ. <	25 Ω 50 Ω
$V_{GS} = 10$ V	r_{DSon}	typ. <	15 Ω 30 Ω
Capacitances at f = 1 MHz (see Fig. 2) $V_{GS} = V_{BS} = -5$ V; $V_{DS} = 10$ V			
Feed-back capacitance	C_{rss}	typ.	0,6 pF
Input capacitance	C_{iss}	typ.	2,3 pF
Output capacitance	C_{oss}	typ.	1,9 pF
Switching times (see Fig. 3) $V_{DD} = 10$ V; $V_i = -5$ to 0 V	t_{on}	typ.	1,0 ns
	t_{off}	typ.	5,0 ns

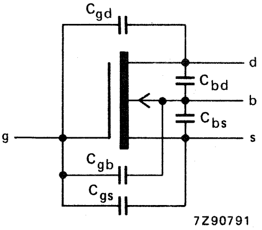


Fig. 2 Capacitances model.

$C_{iss} = C_{gs} + C_{gd} + C_{gb}$
$C_{oss} = C_{gd} + C_{bd}$
$C_{rss} = C_{gd}$

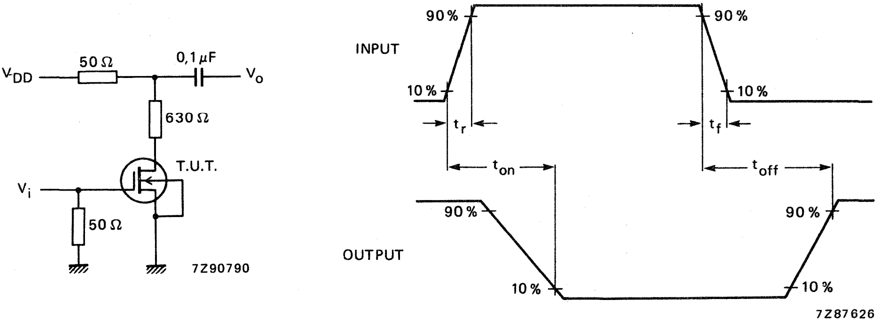


Fig. 3 Switching times and input and output waveforms;
$R_i = 50\ \Omega$; $t_r < 0,5$ ns; $t_f < 1,0$ ns; $t_p = 20$ ns; $\delta < 0,01$.

MOSFET N-CHANNEL DEPLETION SWITCHING TRANSISTORS

Symmetrical insulated-gate silicon MOS field-effect transistors of the N-channel depletion mode type.

The transistor is sealed in a SOT-143 envelope and features a low ON-resistance and low capacitances.

The transistor is protected against excessive input voltages by integrated back-to-back diodes between gate and substrate.

Applications:
- analog and/or digital switch
- switch driver
- convertor
- chopper

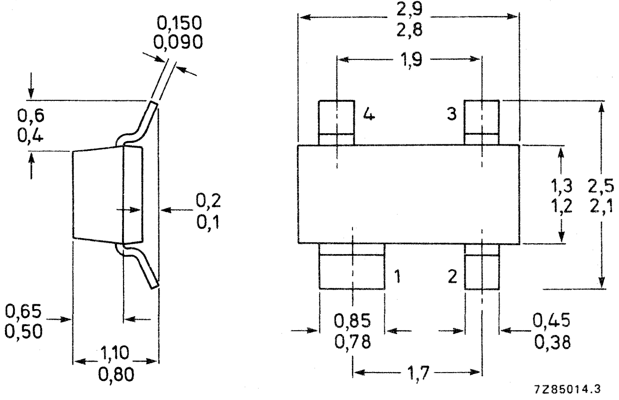
QUICK REFERENCE DATA

			BSD20	BSD22	
Drain-source voltage	V_{DS}	max.	10	20	V
Gate-source voltage	V_{GS}	max.	+10 −30	+20 −40	V V
Drain current (d.c.)	I_D	max.	50		mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	230		mW
Junction temperature	T_j	max.	125		°C
Drain-source ON-resistance V_{GS} = 10 V; V_{SB} = 0; I_D = 1 mA	R_{DSon}	<	30		Ω
Feed-back capacitance $V_{GS} = V_{BS} = -5$ V; V_{DS} = 10 V; f = 1 MHz	C_{rss}	typ.	0,6		pF

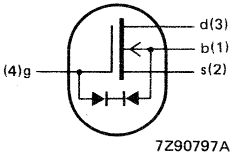
MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-143.



Marking code:
BSD20 = M31
BSD22 = M32



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			BSD20	BSD22	
Drain-source voltage	V_{DS}	max.	10	20	V
Source-drain voltage	V_{SD}	max.	10	20	V
Drain-substrate voltage	V_{DB}	max.	15	25	V
Source-substrate voltage	V_{SB}	max.	15	25	V
Gate-substrate voltage	V_{GB}	max.	± 15	± 25	V
Gate-source voltage	V_{GS}	max.	+ 15 −30	+ 15 −40	V V
Drain current (d.c.)	I_D	max.	50		mA
Total power dissipation up to T_{amb} = 25 °C *	P_{tot}	max.	230		mW
Storage temperature	T_{stg}		−65 to + 150		°C
Junction temperature	T_j	max.	125		°C

THERMAL RESISTANCE

From junction to ambient in free air *	$R_{th\ j\text{-}a}$	=	430	K/W

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

			BSD20	BSD22	
Drain-source breakdown voltage $V_{GS} = V_{BS} = -5$ V; $I_S = 10$ nA	$V_{(BR)DSX}$	>	10	20	V
Source-drain breakdown voltage $V_{GD} = V_{BD} = -5$ V; $I_D = 10$ nA	$V_{(BR)SDX}$	>	10	20	V
Drain-substrate breakdown voltage $V_{GB} = 0$; $I_D = 10$ nA; open source	$V_{(BR)DBO}$	>	15	25	V
Source-substrate breakdown voltage $V_{GB} = 0$; $I_S = 10$ nA; open drain	$V_{(BR)SBO}$	>	15	25	V
Drain-source leakage current $V_{GS} = V_{BS} = -5$ V; $V_{DS} = 20$ V	I_{DSoff}	typ.	1,0		nA
Source-drain leakage current $V_{GD} = V_{BD} = -5$ V; $V_{SD} = 20$ V	I_{SDoff}	typ.	1,0		nA
Gate- substrate leakage current $V_{DB} = V_{SB} = 0$; $V_{GB} = \pm 15$ V	I_{GSoff}	<	10		nA

---

* Device mounted on a ceramic substrate of 8 mm x 10 mm x 0,8 mm.

DEVELOPMENT SAMPLE DATA

Forward transconductance at f = 1 kHz V_{DS} = 10 V; V_{SB} = 0; I_D = 20 mA	g_{fs}	> typ.	10 mS 15 mS
Gate-source cut-off voltage V_{DS} = 10 V; V_{SB} = 0; I_S = 10 μA	$-V_{(P)GS}$	<	2,0 V
Drain-source ON-resistance I_D = 1 mA; V_{SB} = 0; V_{GS} = 5 V	r_{DSon}	typ. <	25 Ω 50 Ω
V_{GS} = 10 V	r_{DSon}	typ. <	15 Ω 30 Ω
Capacitances at f = 1 MHz V_{GS} = V_{BS} = −10 V; V_{DS} = 10 V			
Feed-back capacitance	C_{rss}	typ.	0,6 pF
Input capacitance	C_{iss}	typ.	1,5 pF
Output capacitance	C_{oss}	typ.	1,0 pF
Switching times (see Fig. 2) V_{DD} = 10 V; V_i = 5 V	t_{on} t_{off}	typ. typ.	1,0 ns 5,0 ns

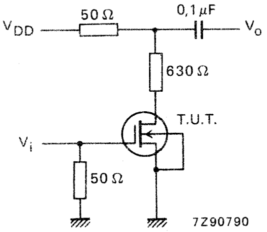


Fig. 2 Switching times test circuit.

MOSFET N-CHANNEL ENHANCEMENT SWITCHING TRANSISTORS

Symmetrical insulated gate silicon MOS field-effect transistor of the N-channel enhancement mode type.

These transistors are hermetically sealed in a TO-72 envelope and feature a low ON-resistance, high switching speed and low capacitances.

The types BSD213 and BSD215 are protected against excessive input voltages by integrated back-to-back diodes between gate and substrate.

Applications:
- analogue and/or digital switch
- switch driver
- converters
- choppers

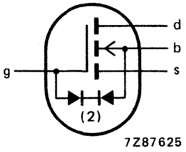
QUICK REFERENCE DATA

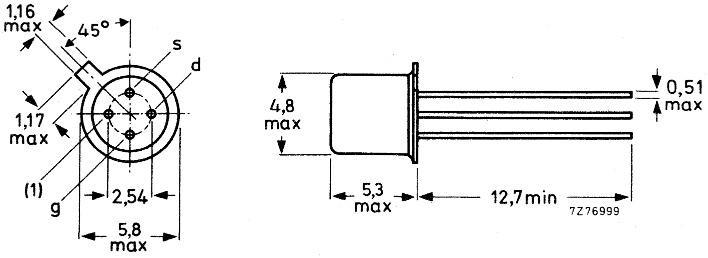
			BSD212	BSD213	BSD214	BSD215	
Drain-source voltage	V_{DS}	max.	10	10	20	20	V
Gate-source voltage	V_{GS}	max.	± 40	+ 15 −30	± 40	+ 15 −40	V
Drain current (d.c.)	I_D	max.	50				mA
Total power dissipation up to T_{amb} = 25 °C (free air)	P_{tot}	max.	275				mW
Drain-source resistance I_D = 1 mA; V_{SB} = 0; V_{GS} = 15 V	r_{DSon}	typ.	25				Ω
Feedback capacitance $V_{GS} = V_{BS} = -15$ V; V_{DS} = 10 V; f = 1 MHz	C_{rss}	typ.	0,6				pF
Junction temperature	T_j	max.	125				°C

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-72.





(1) Substrate (b) connected to case.
(2) Diode protection on types BSD213 and BSD215 only.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			BSD212	BSD213	BSD214	BSD215	
Drain-source voltage	V_{DS}	max.	10	10	20	20	V
Source-drain voltage	V_{SD}	max.	10	10	20	20	V
Drain-substrate voltage	V_{DB}	max.	15	15	25	25	V
Source-substrate voltage	V_{SB}	max.	15	15	25	25	V
Gate-substrate voltage	V_{GB}	max.	± 40	± 15	± 40	± 15	V
Gate-source voltage	V_{GS}	max.	± 40	+ 15 −30	± 40	+ 15 −40	V
Gate-drain voltage	V_{GD}	max.	± 40	+ 15 −30	± 40	+ 15 −40	V
Drain current (d.c.)	I_D	max.	50				mA
Total power dissipation up to T_{amb} = 25 °C (free air)	P_{tot}	max.	275				mW
Storage temperature	T_{stg}		−65 to + 175				°C
Junction temperature	T_j	max.	125				°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	360	K/W

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

			BSD212	BSD213	BSD214	BSD215	
Drain-source breakdown voltage $V_{GS} = V_{BS} = -5$ V; $I_S = 10$ nA	$V_{(BR)DSX}$	>	10	10	20	20	V
Source-drain breakdown voltage $V_{GD} = V_{BD} = -5$ V; $I_D = 10$ nA	$V_{(BR)SDX}$	>	10	10	20	20	V
Drain-substrate breakdown voltage $V_{GB} = 0$; $I_D = 10$ nA; open source	$V_{(BR)DBO}$	>	15	15	25	25	V
Source-substrate breakdown voltage $V_{GB} = 0$; $I_S = 10$ nA; open drain	$V_{(BR)SBO}$	>	15	15	25	25	V
Drain-source leakage current $V_{GS} = V_{BS} = -5$ V; $V_{DS} = 10$ V	I_{DSoff}	typ.	1,0	1,0	–	–	nA
$V_{GS} = V_{BS} = -5$ V; $V_{DS} = 20$ V	I_{DSoff}	typ.	–	–	1,0	1,0	nA
Source-drain leakage current $V_{GD} = V_{BD} = -5$ V; $V_{SD} = 10$ V	I_{SDoff}	typ.	1,0	1,0	–	–	nA
$V_{GD} = V_{BD} = -5$ V; $V_{SD} = 20$ V	I_{SDoff}	typ.	–	–	1,0	1,0	nA
Gate-substrate leakage current $V_{DB} = V_{SB} = 0$; $V_{GB} = \pm 40$ V	I_{GBS}	<	0,1	–	0,1	–	nA
$V_{DB} = V_{SB} = 0$; $V_{GB} = \pm 15$ V	I_{GBS}	<	–	10	–	10	nA
Threshold voltage $V_{DS} = V_{GS} = V_{GS(th)}$ $V_{SB} = 0$; $I_S = 1\ \mu$A	$V_{GS(th)}$		0,1 to 2,0				V

			BSD212	BSD213	BSD214	BSD215	
Drain-source resistance I_D = 1,0 mA; V_{SB} = 0;							
V_{GS} = 5 V	r_{DSon}	typ.	50	50	50	50	Ω
		<	70	70	70	70	Ω
V_{GS} = 10 V	r_{DSon}	typ.	30	30	30	30	Ω
		<	45	45	45	45	
V_{GS} = 15 V	r_{DSon}	typ.	25	25	25	25	Ω
V_{GS} = 25 V	r_{DSon}	typ.	15		15		Ω

DYNAMIC CHARACTERISTICS

Forward transconductance at f = 1 kHz V_{DS} = 10 V; V_{SB} = 0; I_D = 20 mA	g_{fs}	typ.	15	mS
		>	10	
Capacitance at f = 1 MHz (see Fig. 2) V_{GS} = V_{BS} = −15 V; V_{DS} = 10 V				
Feed-back capacitance	C_{rss}	typ.	0,6	pF
Input capacitance	C_{iss}	typ.	2,3	pF
Output capacitance	C_{oss}	typ.	1,9	pF

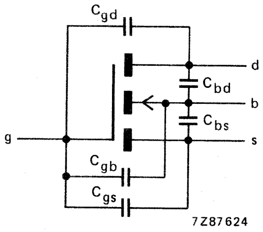


Fig. 2 Capacitances model.

$C_{iss} = C_{GS} + C_{GD} + C_{GB}$

$C_{oss} = C_{GD} + C_{BD}$

$C_{rss} = C_{GD}$

DYNAMIC CHARACTERISTICS (continued)

Switching times (see Fig. 3)

$V_{DD} = 10$ V; $V_i = 5$ V	t_{on}	typ.	1,0	ns
	t_{off}	typ.	5,0	ns

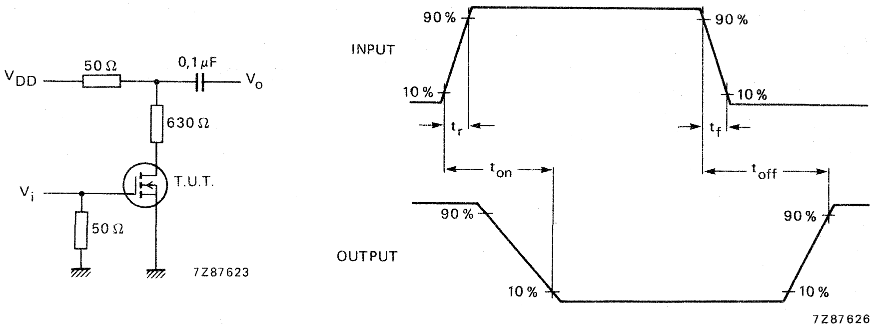


Fig. 3 Switching times test circuit and input and output waveforms.

Pulse generator:

$R_i = 50\ \Omega$

$t_r < 0{,}5$ ns

$t_f < 1{,}0$ ns

$t_p = 20$ ns

$\delta < 0{,}01$

MOSFET N-CHANNEL ENHANCEMENT SWITCHING TRANSISTOR

Symmetrical insulated-gate silicon MOS field-effect transistor of the N-channel enhancement mode type.

The transistor is sealed in a SOT-143 envelope and features a low ON resistance and low capacitances.

The transistor is protected against excessive input voltages by integrated back-to-back diodes between gate and substrate.

Applications:
- analog and/or digital switch
- switch driver

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	10	V
Source-drain voltage	V_{SD}	max.	10	V
Drain-substrate voltage	V_{DB}	max.	15	V
Source-substrate voltage	V_{SB}	max.	15	V
Drain current (d.c.)	I_D	max.	50	mA
Total power dissipation up to $T_{amb} = 25\ ^{o}C$	P_{tot}	max.	230	mW
Gate-source cut-off voltage $V_{DS} = V_{GS}$; $V_{SB} = 0$; $I_D = 1\ \mu A$	$V_{(P)GS}$	> <	0,1 2,0	V V
Drain-source ON-resistance $V_{GS} = 10$ V; $V_{SB} = 0$; $I_D = 0,1$ mA	r_{DSon}	<	45	Ω
Feed-back capacitance $V_{GS} = V_{BS} = -15$ V; $V_{DS} = 10$ V; f = 1 MHz	C_{rss}	typ.	0,6	pF

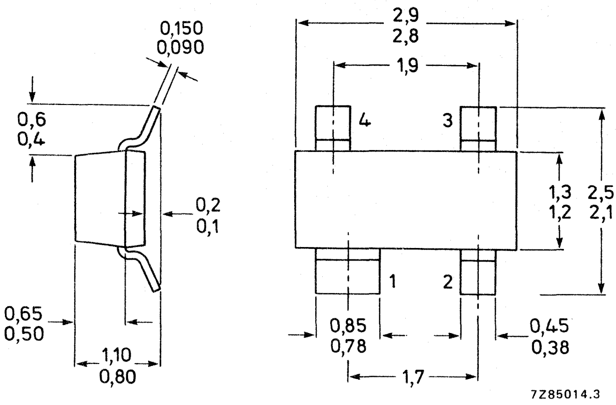
MECHANICAL DATA

SOT-143 (see Fig. 1).

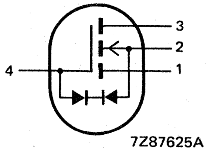
See also *Soldering recommendations*.

Fig. 1 SOT-143.

Dimensions in mm



Marking code:
BSS83 = M74



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	10 V
Source-drain voltage	V_{SD}	max.	10 V
Drain-substrate voltage	V_{DB}	max.	15 V
Source-substrate voltage	V_{SB}	max.	15 V
Drain current (d.c.)	I_D	max.	50 mA
Total power dissipation up to T_{amb} = 25 °C*	P_{tot}	max.	230 mW*
Storage temperature	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	125 °C

THERMAL RESISTANCE

From junction to ambient in free air*	$R_{th\ j\text{-}a}$	=	430 K/W*

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

Drain-source breakdown voltage $V_{GS} = V_{BS} = -5$ V; I_D = 10 nA	$V_{(BR)DSX}$	>	10 V
Source-drain breakdown voltage $V_{GD} = V_{BD} = -5$ V; I_D = 10 nA	$V_{(BR)SDX}$	>	10 V
Drain-substrate breakdown voltage V_{CB} = 0; I_D = 10 nA; open source	$V_{(BR)DBO}$	>	15 V
Source-substrate breakdown voltage V_{CB} = 0; I_D = 10 nA; open drain	$V_{(BR)SBO}$	>	15 V
Drain-source leakage current $V_{GS} = V_{BS} = -2$ V; V_{DS} = 6,6 V	I_{DSoff}	<	10 nA

* Device mounted on a ceramic substrate of 8 mm x 10 mm x 0,6 mm.

Source-drain leakage current $V_{GD} = V_{BD} = -2$ V; $V_{SD} = 6,6$ V	I_{SDoff}	<	10 mA
Forward transconductance at f = 1 kHz $V_{DS} = 10$ V; $V_{SB} = 0$; $I_D = 20$ mA	g_{fs}	> typ.	10 mS 15 mS
Gate-source cut-off voltage $V_{DS} = V_{GS}$; $V_{SB} = 0$; $I_D = 1$ μA	$V_{(P)GS}$	> <	0,1 V 2,0 V
Drain-source ON-resistance $I_D = 0,1$ mA;			
$V_{GS} = 5$ V; $V_{SB} = 0$	r_{DSon}	<	70 Ω
$V_{GS} = 10$ V; $V_{SB} = 0$	r_{DSon}	<	45 Ω
$V_{GS} = 3,2$ V; $V_{SB} = 6,8$ V	r_{DSon}	typ. <	80 Ω 120 Ω
Gate-substrate zener voltages $V_{DB} = V_{SB} = 0$; $-I_C = 10$ μA	$V_{Z(1)}$	>	12,5 V
$V_{DB} = V_{SB} = 0$; $+I_G = 10$ μA	$V_{Z(2)}$	>	12,5 V
Capacitances at f = 1 MHz $V_{GS} = V_{BS} = -15$ V; $V_{DS} = 10$ V			
Feed-back capacitance	C_{rss}	typ.	0,6 pF
Input capacitance	C_{iss}	typ.	1,5 pF
Output capacitance	C_{oss}	typ.	1,0 pF
Switching times (see Fig. 2) $V_{DD} = 10$ V; $V_i = 5$ V	t_{on}	typ.	1,0 ns
	t_{off}	typ.	5,0 ns

Pulse generator:
$R_i = 50$ Ω
$t_r < 0,5$ ns
$t_f < 1,0$ ns
$t_p = 20$ ns
$\delta < 0,01$

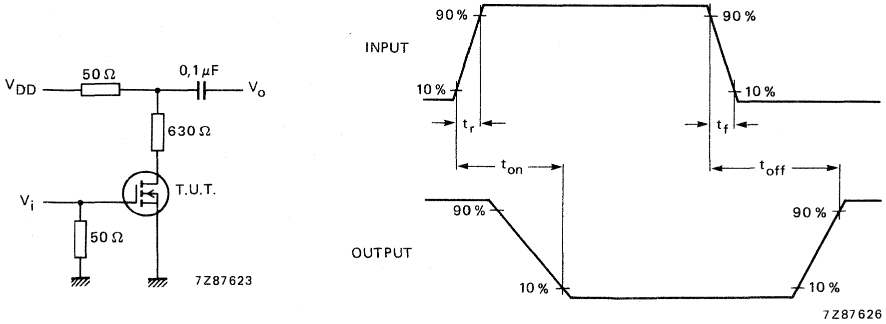


Fig. 2 Switching times test circuit and input and output waveforms.

N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

Features:

- Very low R_{DSon}
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

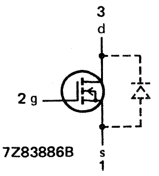
QUICK REFERENCE DATA

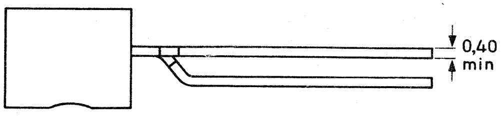
Drain-source voltage	V_{DS}	max.	80	V
Gate-source voltage (open drain)	V_{GSO}	max.	20	V
Drain current (d.c.)	I_D	max.	0,5	A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Drain-source ON-resistance I_D = 500 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	2 4	Ω Ω
Transfer admittance I_D = 500 mA; V_{DS} = 15 V; f = 1 kHz	$\lvert y_{fs} \rvert$	typ.	300	mS

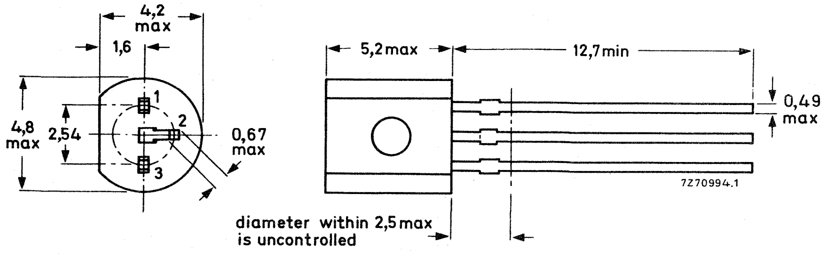
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.







RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	80	V
Gate-source voltage (open drain)	V_{GSO}	max.	20	V
Drain current (d.c.)	I_D	max.	0,5	A
Drain current (peak)	I_{DM}	max.	1,0	A
Total power dissipation up to T_{amb} = 25 °C*	P_{tot}	max.	1	W
Storage temperature	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient*	$R_{th\ j\text{-}a}$	125	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 100 μA; V_{GS} = 0	$V_{(BR)DS}$	>	80	V
Drain-source leakage current V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	<	10	μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	<	100	nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	>	1,5	V
		<	3,5	V
Drain-source ON-resistance (see Fig. 4) I_D = 500 mA; V_{GS} = 10 V	R_{DSon}	typ.	2,0	Ω
		<	4,0	Ω
Transfer admittance at f = 1 kHz I_D = 500 mA; V_{DS} = 15 V	$\lvert y_{fs} \rvert$	typ.	300	mS
Input capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{is}	typ.	45	pF
Output capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{os}	typ.	30	pF
Feedback capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{rs}	typ.	8	pF
Switching times (see Figs 2 and 3) I_D = 500 mA; V_{DS} = 50 V; V_{GS} = 0 to 10 V	t_{on}	<	10	ns
	t_{off}	<	15	ns

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* Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm x 10 mm.

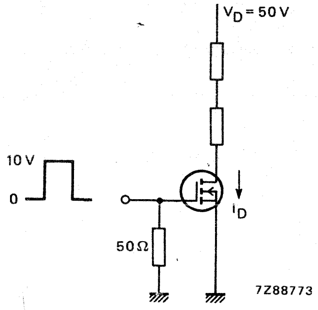


Fig. 2 Switching times test circuit.

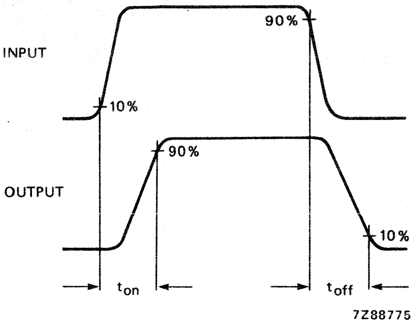


Fig. 3 Input and output waveforms.

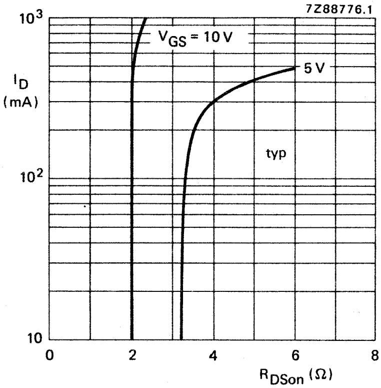


Fig. 4 $T_j = 25\ ^oC$.

N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and designed for use in telephone ringer circuits and for application with relay, high-speed and line-transformer drivers.

Features:

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

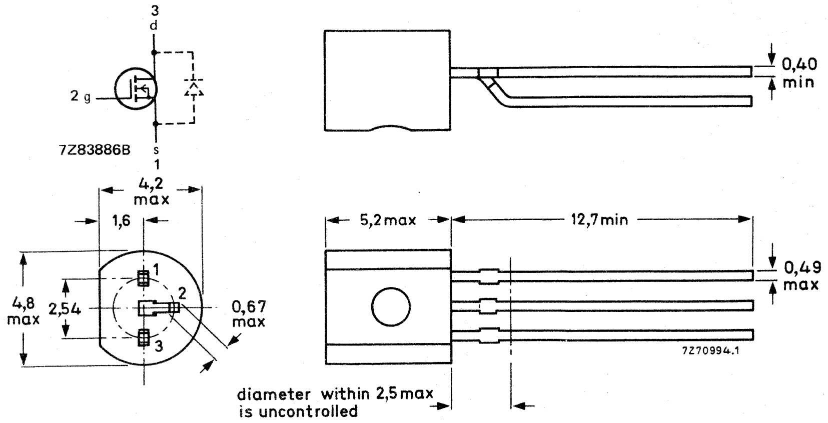
QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	80	V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 2$ ms)	$V_{DS(SM)}$	max.	100	V
Gate-source voltage (open drain)	V_{GSO}	max.	20	V
Drain current (d.c.)	I_D	max.	300	mA
Total power dissipation up to $T_{amb} = 25$ °C	P_{tot}	max.	0,83	W
Drain-source ON-resistance $I_D = 150$ mA; $V_{GS} = 5$ V	R_{DSon}	typ. max.	7 10	Ω Ω
Transfer admittance $I_D = 200$ mA; $V_{DS} = 5$ V; f = 1 kHz	$\lvert y_{fs} \rvert$	typ.	150	mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	80	V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 2$ ms)	$V_{DS(SM)}$	max.	100	V
Gate-source voltage (open drain)	V_{GSO}	max.	20	V
Drain current (d.c.)	I_D	max.	300	mA
Drain current (peak)	I_{DM}	max.	600	mA
Total power dissipation up to T_{amb} = 25 °C*	P_{tot}	max.	0,83	W
Storage temperature	T_{stg}	−65 to +	150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient*	$R_{th\ j\text{-}a}$		150	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 100 μA; V_{GS} = 0	$V_{(BR)DS}$	>	80	V
Drain-source leakage current V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	<	1,0	μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	<	100	nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	> <	1,5 3,5	V V
Drain-source ON-resistance (see Fig. 4) I_D = 150 mA; V_{GS} = 5 V	R_{DSon}	typ. <	7 10	Ω Ω
Transfer admittance at f = 1 kHz I_D = 200 mA; V_{DS} = 5 V	$\|y_{fs}\|$	typ.	150	mS
Input capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{is}	typ.	15	pF
Output capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{os}	typ.	13	pF
Feedback capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{rs}	typ.	3	pF
Switching times (see Figs 2 and 3) I_D = 200 mA; V_{DS} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ. <	4 10	ns ns
	t_{off}	typ. <	4 10	ns ns

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* Transistor mounted on printed circuit board, max. lead length 4 mm.

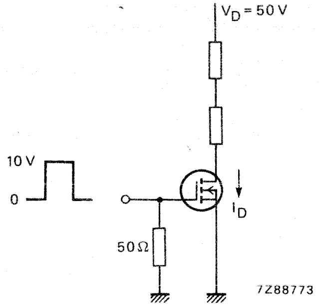


Fig. 2 Switching times test circuit.

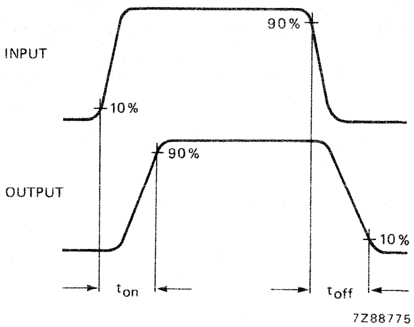


Fig. 3 Input and output waveforms.

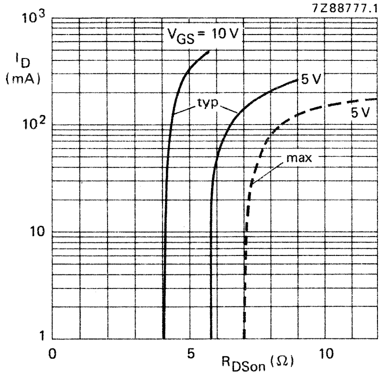


Fig. 4 $T_j = 25$ °C.

N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and designed for use as line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features:

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

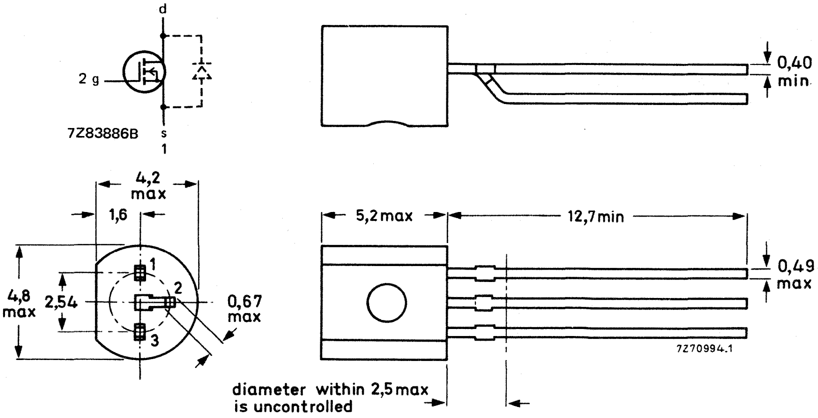
QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200	V
Gate-source voltage (open drain)	V_{GSO}	max.	20	V
Drain current (d.c.)	I_D	max.	300	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Drain-source ON-resistance I_D = 400 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	6 12	Ω Ω
Transfer admittance I_D = 400 mA; V_{DS} = 15 V; f = 1 kHz	$\lvert y_{fs} \rvert$	typ.	250	mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	V_{GSO}	max.	20 V
Drain current (d.c.)	I_D	max.	300 mA
Drain current (peak)	I_{DM}	max.	800 mA
Total power dissipation up to T_{amb} = 25 °C*	P_{tot}	max.	1 W
Storage temperature	T_{stg}	−65 to + 150 °C	
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient*	$R_{th\ j\text{-}a}$		125 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 100 μA; V_{GS} = 0	$V_{(BR)DS}$	>	200 V
Drain-source leakage current V_{DS} = 160 V; V_{GS} = 0	I_{DSS}	<	10 μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	<	100 nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	> <	1,5 V 3,5 V
Drain-source ON-resistance (see Fig. 4) I_D = 400 mA; V_{GS} = 10 V	R_{DSon}	typ. <	6 Ω 12 Ω
Transfer admittance at f = 1 kHz I_D = 400 mA; V_{DS} = 15 V	$\lvert y_{fs} \rvert$	typ.	250 mS
Input capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{is}	typ.	40 pF
Output capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{os}	typ.	20 pF
Feedback capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{rs}	typ.	6 pF
Switching times (see Figs 2 and 3) I_D = 400 mA; V_{DS} = 50 V; V_{GS} = 0 to 10 V	t_{on} t_{off}	< <	10 ns 15 ns

* Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for collector lead min. 10 mm x 10 mm.

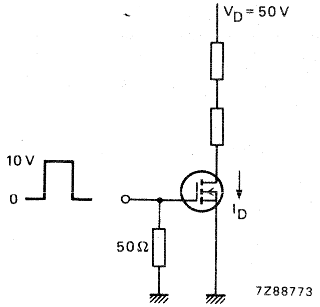


Fig. 2 Switching times test circuit.

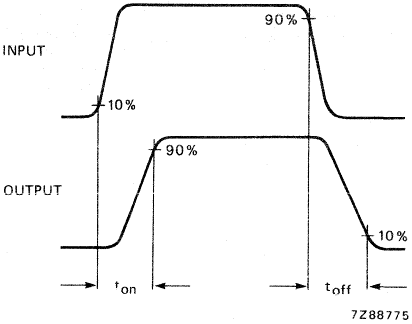


Fig. 3 Input and output waveforms.

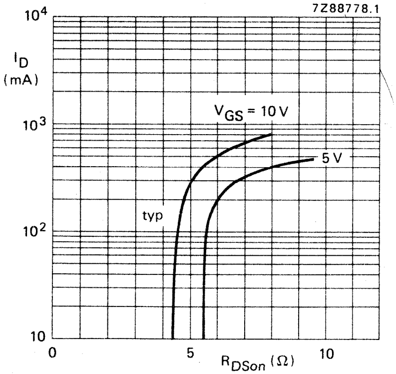


Fig. 4 $T_j = 25\ ^{o}C$.

N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and designed for use as line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features:

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

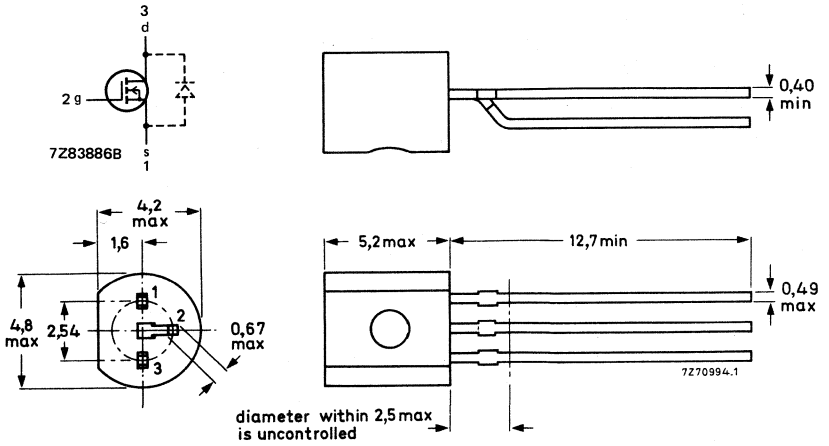
QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	180	V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 2$ ms)	$V_{DS(SM)}$	max.	200	V
Gate-source voltage (open drain)	V_{GSO}	max.	20	V
Drain current (d.c.)	I_D	max.	300	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Drain-source ON-resistance I_D = 15 mA; V_{GS} = 3 V	R_{DSon}	typ. max.	7 10	Ω Ω
Transfer admittance I_D = 400 mA; V_{DS} = 15 V; f = 1 kHz	$\lvert y_{fs} \rvert$	typ.	250	mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	180	V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 2$ ms)	$V_{DS(SM)}$	max.	200	V
Gate source voltage (open drain)	V_{GSO}	max.	20	V
Drain current (d.c.)	I_D	max.	300	mA
Drain current (peak)	I_{DM}	max.	800	mA
Total power dissipation up to $T_{amb} = 25$ °C*	P_{tot}	max.	1	W
Storage temperature	T_{stg}	−65 to +	150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient*	$R_{th\,j\text{-}a}$		125	K/W

CHARACTERISTICS

$T_j = 25$ °C unless otherwise specified

Drain-source breakdown voltage $I_D = 100\ \mu A$; $V_{GS} = 0$	$V_{(BR)DS}$	>	180	V
Drain-source leakage current $V_{DS} = 120$ V; $V_{GS} = 0$	I_{DSS}	<	10	μA
Gate-source leakage current $V_{GS} = 20$ V; $V_{DS} = 0$	I_{GSS}	<	100	nA
Gate threshold voltage $I_D = 100\ \mu A$; $V_{DS} = V_{GS}$	$V_{GS(th)}$	>	0,7	V
		<	2,7	V
Drain-source ON-resistance (see Fig. 4) $I_D = 15$ mA; $V_{GS} = 3$ V	R_{DSon}	typ.	7	Ω
		<	10	Ω
$I_D = 400$ mA; $V_{GS} = 10$ V	R_{DSon}	typ.	6	Ω
Transfer admittance at f = 1 kHz $I_D = 400$ mA; $V_{DS} = 15$ V	$\lvert y_{fs} \rvert$	typ.	250	mS
Input capacitance at f = 1 MHz $V_{DS} = 10$ V; $V_{GS} = 0$	C_{is}	typ.	50	pF
Output capacitance at f = 1 MHz $V_{DS} = 10$ V; $V_{GS} = 0$	C_{os}	typ.	20	pF
Feedback capacitance at f = 1 MHz $V_{DS} = 10$ V; $V_{GS} = 0$	C_{rs}	typ.	6	pF
Switching times (see Figs 2 and 3) $I_D = 400$ mA; $V_{DS} = 50$ V; $V_{GS} = 0$ to 10 V	t_{on}	<	10	ns
	t_{off}	<	15	ns

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* Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm x 10 mm.

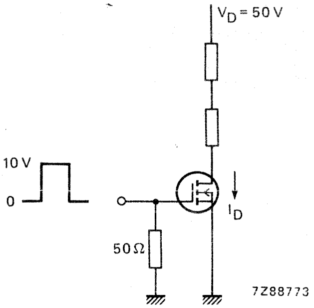


Fig. 2 Switching times test circuit.

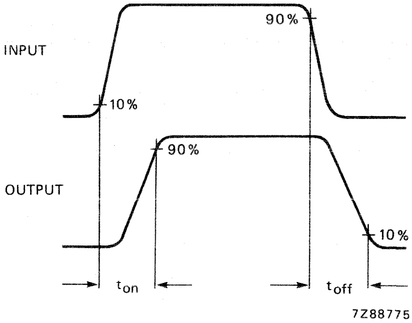


Fig. 3 Input and output waveforms.

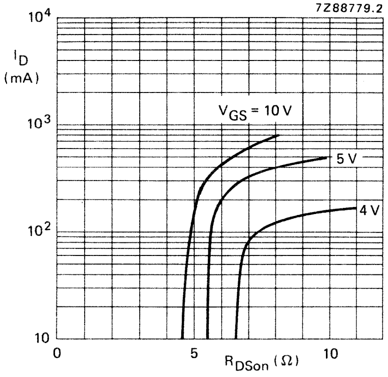


Fig. 4 T_j = 25 °C; typ. values.

HIGH-VOLTAGE N-CHANNEL VERTICAL D-MOS TRANSISTOR

High-voltage N-channel vertical D-MOS transistor in plastic TO-126 envelope and intended for use in relay, high-speed and line-transformer drivers.

Features:

- Direct interface to C-MOS, TTL, etc.
- High-speed switching, low power switching losses
- No second breakdown

QUICK REFERENCE DATA

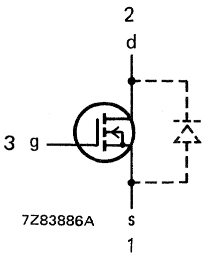
Drain-source voltage	V_{DS}	max.	450	V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 50\ \mu s$)	$V_{DS(SM)}$	max.	525	V
Gate-source voltage (open drain)	V_{GSO}	max.	20	V
Drain current (d.c.)	I_D	max.	0,75	A
Total power dissipation up to $T_{mb} = 75\ ^oC$	P_{tot}	max.	15	W
Drain-source ON-resistance $I_D = 500$ mA; $V_{GS} = 10$ V	R_{DSon}	typ.	15	Ω
Transfer admittance $I_D = 250$ mA; $V_{DS} = 20$ V; f = 1 kHz	$\lvert y_{fs} \rvert$	typ.	400	mS

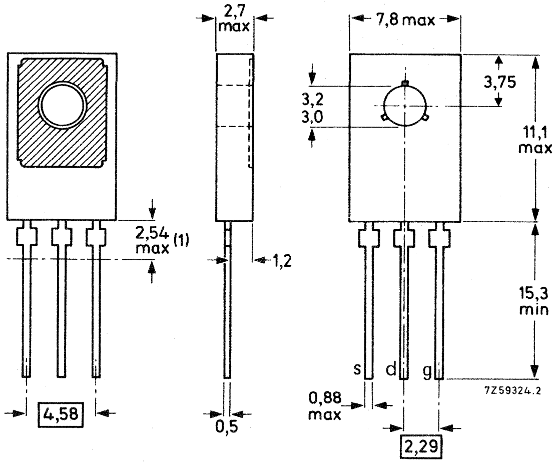
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-126.

Drain connected to mounting base.





RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	450	V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 50\ \mu s$)	V	max.	525	V
Gate-source voltage (open drain)	V_{GSO}	max.	20	V
Drain current (d.c.)	I_D	max.	0,75	A
Drain current (peak)	I_{DM}	max.	1,5	A
Total power dissipation up to $T_{mb} = 75\ ^oC$	P_{tot}	max.	15	W
Storage temperature	T_{stg}	−65 to	+150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	100	K/W
From junction to mounting base	$R_{th\ j\text{-}mb}$	5	K/W

CHARACTERISTICS

$T_j = 25\ ^oC$ unless otherwise specified

Drain-source breakdown voltage $I_D = 100\ \mu A$; $V_{GS} = 0$	$V_{(BR)DS}$	>	450	V
Drain-source leakage current $V_{DS} = 350$ V; $V_{GS} = 0$	I_{DSS}	<	25	μA
Gate-source leakage current $V_{GS} = 20$ V; $V_{DS} = 0$	I_{GSS}	<	100	nA
Gate-source cut-off voltage $I_D = 1$ mA; $V_{DS} = V_{GS}$	$V_{(P)GS}$	> <	2,0 4,0	V V
Drain-source ON-resistance (see Fig. 4) $I_D = 100$ mA; $V_{GS} = 10$ V	R_{DSon}	typ. <	10 14	Ω Ω
$I_D = 500$ mA; $V_{GS} = 10$ V	R_{DSon}	typ.	15	Ω
Transfer admittance at f = 1 kHz $I_D = 250$ mA; $V_{DS} = 20$ V	$\lvert y_{fs} \rvert$	typ.	400	mS
Input capacitance at f = 1 MHz $V_{DS} = 10$ V; $V_{GS} = 0$	C_{is}	typ. <	75 100	pF pF
Output capacitance at f = 1 MHz $V_{DS} = 10$ V; $V_{GS} = 0$	C_{os}	typ. <	25 35	pF pF
Feedback capacitance at f = 1 MHz $V_{DS} = 10$ V; $V_{GS} = 0$	C_{rs}	typ. <	3 5	pF pF
Switching times (see Figs 2 and 3) $I_D = 100$ mA; $V_{DS} = 200$ V; $V_{GS} = 0$ to 10 V	t_{on}	<	10	ns
	t_{off}	<	100	ns

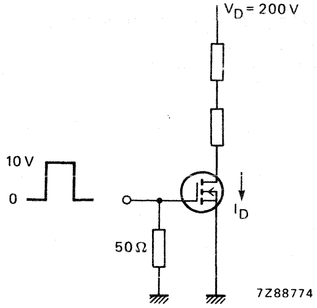


Fig. 2 Switching times test circuit.

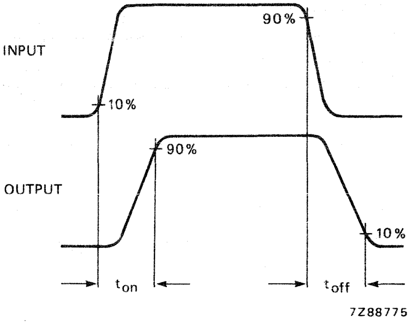


Fig. 3 Input and output waveforms.

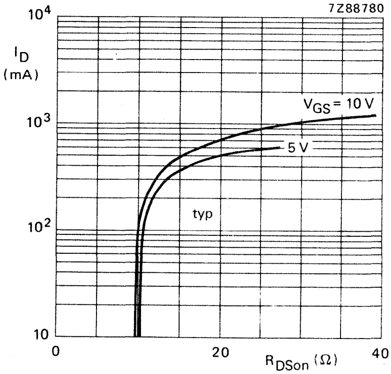


Fig. 4 $T_j = 25\ ^oC$.

N-CHANNEL IG-MOS-FET

Symmetrical depletion type field-effect transistor in a TO-72 metal envelope with the substrate connected to the case. It is intended for chopper and other special switching applications, e.g. timing circuits, multiplex circuits, etc. The features are a very low drain-source 'on' resistance, a very high drain-source 'off' resistance and low feedback capacitances.

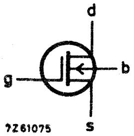
QUICK REFERENCE DATA

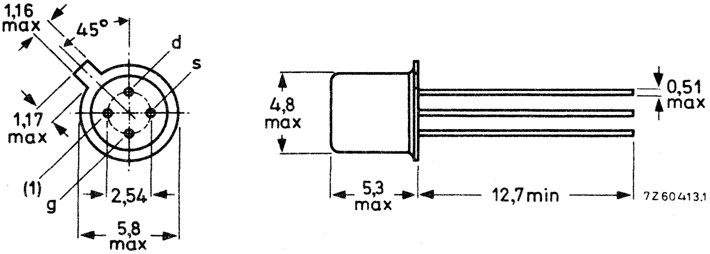
Drain-source resistance (on) at f = 1 kHz $V_{DS} = 0$; $V_{GS} = 5$ V; $V_{BS} = 0$	$r_{ds\,on}$	<	50 Ω
Drain-source resistance (off) $V_{DS} = 10$ V; $-V_{GS} = 5$ V; $V_{BS} = 0$	r_{DSoff}	>	10 GΩ
Feedback capacitance at f = 1 MHz $-V_{GS} = 5$ V; $V_{DS} = 0$; $I_B = 0$	C_{rs}	<	0,5 pF
$-V_{GD} = 5$ V; $V_{SD} = 0$; $I_B = 0$	C_{rd}	<	0,5 pF

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-72.





(1) = substrate connected to case.

Accessories: 56246 (distance disc).

Note
To safeguard the gates against damage due to accumulation of static charge during transport or handling, the leads are encircled by a ring of conductive rubber which should be removed just after the transistor is soldered into the circuit.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages

Drain-substrate voltage	V_{DB}	max.	30	V
Source-substrate voltage	V_{SB}	max.	30	V
Gate-substrate voltage (continuous)	V_{GB}	max. min.	10 −10	V V
Repetitive peak gate to all other terminals voltage $V_{SB} = V_{DB} = 0$; $f > 100$ Hz	$V_{G\text{-}N}$	max. min.	15 −15	V V
Non-repetitive peak gate to all other terminals voltage $V_{SB} = V_{DB} = 0$; $t < 10$ ms	$V_{G\text{-}N}$	max. min.	50 −50	V V

Currents

Drain current (peak value) $t_r = 20$ ms; $\delta = 0,1$	I_{DM}	max.	50	mA
Source current (peak value) $t_r = 20$ ms; $\delta = 0,1$	I_{SM}	max.	50	mA

Power dissipation

Total power dissipation up to $T_{amb} = 25$ °C	P_{tot}	max.	200	mW

Temperatures

Storage temperature	T_{stg}	−65 to +125		°C
Junction temperature	T_j	max.	125	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	0,5	°C/mW

CHARACTERISTICS

$T_j = 25\ ^{o}C$ unless otherwise specified

Drain cut-off currents; $V_{BS} = 0$

$V_{DS} = 10$ V; $-V_{GS} = 5$ V	I_{DSX}	<	1	nA
$V_{DS} = 10$ V; $-V_{GS} = 5$ V; $T_j = 125\ ^{o}C$	I_{DSX}	<	1	μA

Source cut-off currents; $V_{BD} = 0$

$V_{SD} = 10$ V; $-V_{GD} = 5$ V	I_{SDX}	<	1	nA
$V_{SD} = 10$ V; $-V_{GD} = 5$ V; $T_j = 125\ ^{o}C$	I_{SDX}	<	1	μA

Gate currents; $V_{BS} = 0$

$-V_{GS} = 10$ V; $V_{DS} = 0$	$-I_{GSS}$	<	10	pA
$V_{GS} = 10$ V; $V_{DS} = 0$	I_{GSS}	<	10	pA
$-V_{GS} = 10$ V; $V_{DS} = 0$; $T_j = 125\ ^{o}C$	$-I_{GSS}$	<	200	pA
$V_{GS} = 10$ V; $V_{DS} = 0$; $T_j = 125\ ^{o}C$	I_{GSS}	<	200	pA

Bulk currents; $V_{GB} = 0$

$-V_{BD} = 30$ V; $I_S = 0$	$-I_{BDO}$	<	10	μA
$-V_{BS} = 30$ V; $I_D = 0$	$-I_{BSO}$	<	10	μA

Drain-source resistance (on) at f = 1 kHz; $V_{BS} = 0$

$V_{GS} = 0$; $V_{DS} = 0$	$r_{ds\,on}$	<	100	Ω
$V_{GS} = 0$; $V_{DS} = 0$; $T_j = 125\ ^{o}C$	$r_{ds\,on}$	<	150	Ω
$+V_{GS} = 5$ V; $V_{DS} = 0$	$r_{ds\,on}$	<	50	Ω

Drain-source resistance (off)

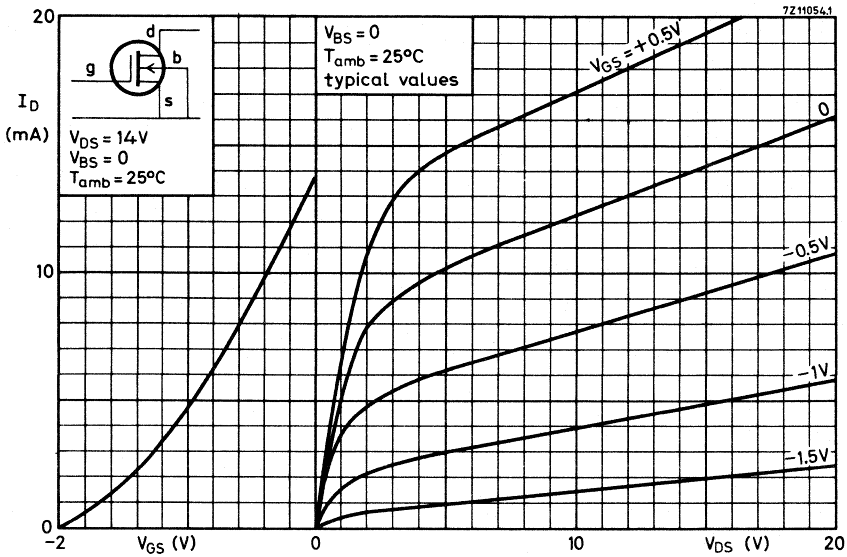
$-V_{GS} = 5$ V; $V_{DS} = 10$ V; $V_{BS} = 0$	r_{DSoff}	>	10	GΩ

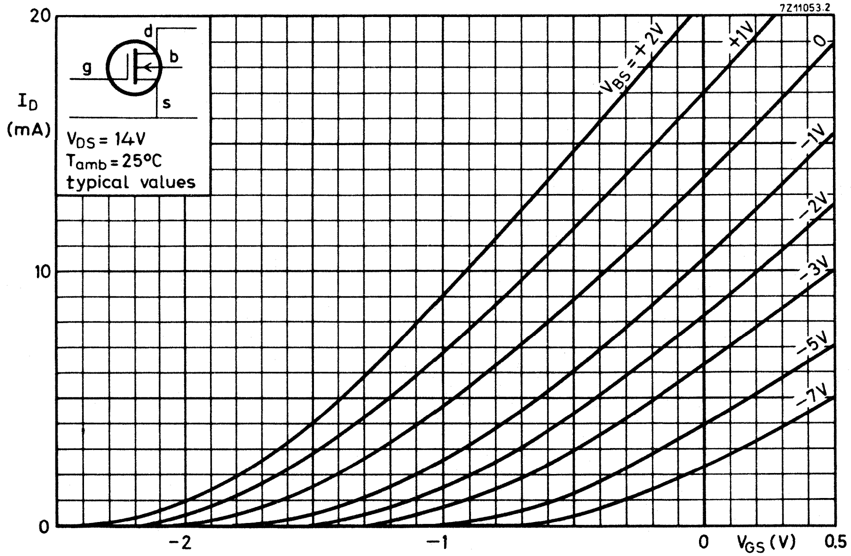
Feedback capacitances at f = 1 MHz

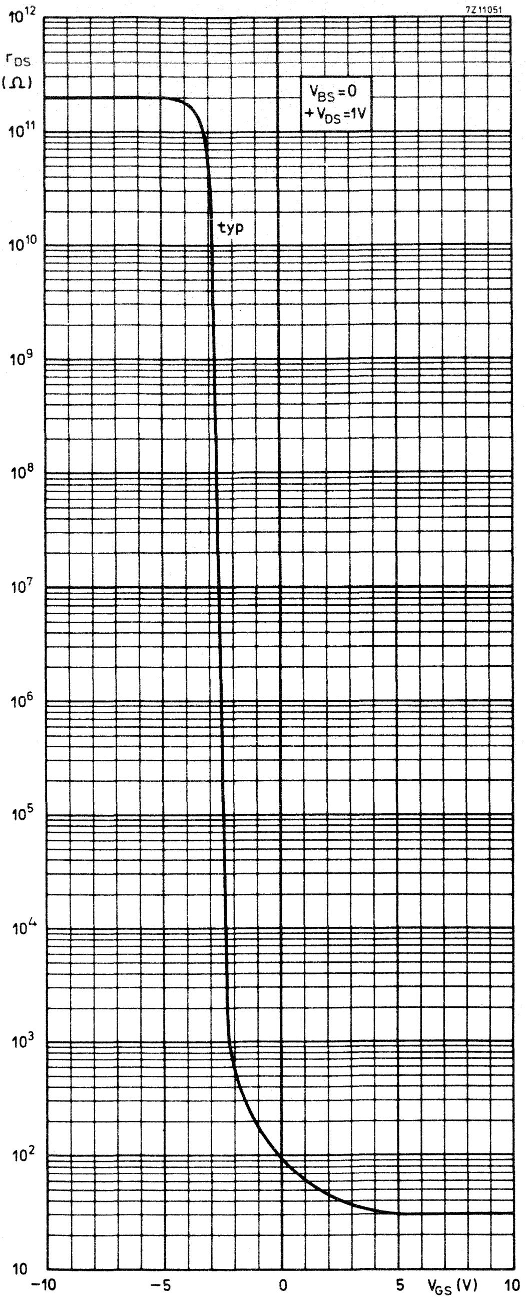
$-V_{GS} = 5$ V; $V_{DS} = 0$; $I_B = 0$	C_{rs}	<	0,5	pF
$-V_{GD} = 5$ V; $V_{SD} = 0$; $I_B = 0$	C_{rd}	<	0,5	pF

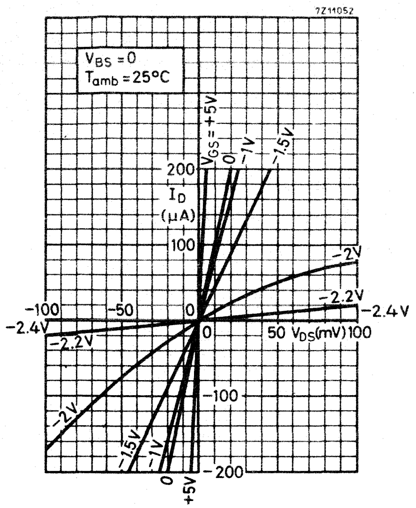
Gate to all other terminals capacitance at f = 1 MHz

$-V_{GB} = 5$ V; $V_{SB} = V_{DB} = 0$	C_{g-n}	<	6	pF


7Z11054.1
20
10
0
I_D
(mA)
d
g
b
s
V_{DS} = 14V
V_{BS} = 0
T_{amb} = 25°C
V_{BS} = 0
T_{amb} = 25°C
typical values
V_{GS} = +0.5V
0
−0.5V
−1V
−1.5V
−2
V_{GS} (V)
0
10
V_{DS} (V)
20


7Z11053.2
20
10
0
I_D
(mA)
d
g
b
s
V_{DS} = 14V
T_{amb} = 25°C
typical values
V_{BS} = +2V
+1V
0
−1V
−2V
−3V
−5V
−7V
−2
−1
0
V_{GS} (V)
0.5


7Z11051
10^12
r_DS
(Ω)
10^11
10^10
10^9
10^8
10^7
10^6
10^5
10^4
10^3
10^2
10
V_BS = 0
+V_DS = 1V
typ
−10
−5
0
5
V_GS (V)
10


7Z11052
V_BS = 0
T_amb = 25°C
V_GS = +5V
0
−1V
−1.5V
200
I_D
(μA)
100
−2V
−2.2V
−2.4V
−100
−50
0
0
50
V_DS(mV)
100
−2.4V
−2.2V
−100
−2V
−1.5V
−1V
0
+5V
−200

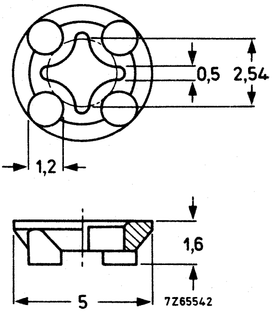
DISTANCE DISC

MECHANICAL DATA

Dimensions in mm

Fig. 2 **56246** for **TO-18** or **TO-72**

Insulating material.



TEMPERATURE

Maximum permissible temperature	T	max. 100 °C

INDEX OF TYPE NUMBERS

Data Handbooks Semiconductor Devices

type no.	book	section	type no.	book	section	type no.	book	section
AA119	S1	GD	BAS19	S7/S1	Mm/SD	BB109G	S1	T
AAZ15	S1	GD	BAS20	S7/S1	Mm/SD	BB112	S1	T
AAZ17	S1	GD	BAS21	S7/S1	Mm/SD	BB119	S1	T
AAZ18	S1	GD	BAT17	S7/S1	Mm/T	BB130	S1	T
BA220	S1	SD	BAT18	S7/S1	Mm/T	BB204B	S1	T
BA221	S1	SD	BAT81	S1	T	BB204G	S1	T
BA223	S1	T	BAT82	S1	T	BB212	S1	T
BA243	S1	T	BAT83	S1	T	BB405B	S1	T
BA244	S1	T	BAT85	S1	T	BB405G	S1	T
BA280	S1	T	BAV10	S1	SD	BB417	S1	T
BA314	S1	Vrg	BAV18	S1	SD	BB809	S1	T
BA315	S1	Vrg	BAV19	S1	SD	BB909A	S1	T
BA316	S1	SD	BAV20	S1	SD	BB909B	S1	T
BA317	S1	SD	BAV21	S1	SD	BBY31	S7/S1	Mm/T
BA318	S1	SD	BAV45	S1	Sp	BBY40	S7/S1	Mm/T
BA379	S1	T	BAV70	S7/S1	Mm/SD	BC107	S3	Sm
BA423	S1	T	BAV99	S7/S1	Mm/SD	BC108	S3	Sm
BA481	S1	T	BAW56	S7/S1	Mm/SD	BC109	S3	Sm
BA482	S1	T	BAW62	S1	SD	BC146	S3	Sm
BA483	S1	T	BAX12	S1	SD	BC177	S3	Sm
BA484	S1	T	BAX12A	S1	SD	BC178	S3	Sm
BAS11	S1	SD	BAX14	S1	SD	BC179	S3	Sm
BAS16	S7/S1	Mm/SD	BAX18	S1	SD	BC200	S3	Sm
BAS17	S7/S1	Mm/Vrg	BB105B	S1	T	BC264A	S5	FET
BAS18	S1	SD	BB105G	S1	T	BC264B	S5	FET

FET = Field-effect transistors
GD = Germanium diodes
Mm = Microminiature semiconductors for hybrid circuits
SD = Small-signal diodes

Sm = Small-signal transistors
Sp = Special diodes
T = Tuner diodes
Vrg = Voltage regulator diodes

type no.	book	section
BC264C	S5	FET
BC264D	S5	FET
BC327;A	S3	Sm
BC328	S3	Sm
BC337;A	S3	Sm
BC338	S3	Sm
BC368	S3	Sm
BC369	S3	Sm
BC375	S3	Sm
BC376	S3	Sm
BC546	S3	Sm
BC547	S3	Sm
BC548	S3	Sm
BC549	S3	Sm
BC550	S3	Sm
BC556	S3	Sm
BC557	S3	Sm
BC558	S3	Sm
BC559	S3	Sm
BC560	S3	Sm
BC635	S3	Sm
BC636	S3	Sm
BC637	S3	Sm
BC638	S3	Sm
BC639	S3	Sm
BC640	S3	Sm
BC807	S7	Mm
BC808	S7	Mm
BC817	S7	Mm
BC818	S7	Mm
BC846	S7	Mm
BC847	S7	Mm
BC848	S7	Mm
BC849	S7	Mm
BC850	S7	Mm
BC856	S7	Mm
BC857	S7	Mm
BC858	S7	Mm
BC859	S7	Mm
BC860	S7	Mm
BC868	S7	Mm
BC869	S7	Mm
BCF29;R	S7	Mm
BCF30;R	S7	Mm
BCF32;R	S7	Mm
BCF33;R	S7	Mm
BCF70;R	S7	Mm
BCF81;R	S7	Mm
BCV71;R	S7	Mm
BCV72;R	S7	Mm
BCW29;R	S7	Mm
BCW30;R	S7	Mm
BCW31;R	S7	Mm
BCW32;R	S7	Mm
BCW33;R	S7	Mm
BCW60*	S7	Mm
BCW61*	S7	Mm
BCW69;R	S7	Mm
BCW70;R	S7	Mm
BCW71;R	S7	Mm
BCW72;R	S7	Mm
BCW81;R	S7	Mm
BCW89;R	S7	Mm
BCX17;R	S7	Mm
BCX18;R	S7	Mm
BCX19;R	S7	Mm
BCX20;R	S7	Mm
BCX51	S7	Mm
BCX52	S7	Mm
BCX53	S7	Mm
BCX54	S7	Mm
BCX55	S7	Mm
BCX56	S7	Mm
BCX70*	S7	Mm
BCX71*	S7	Mm
BCY56	S3	Sm
BCY57	S3	Sm
BCY58	S3	Sm
BCY59	S3	Sm
BCY70	S3	Sm
BCY71	S3	Sm
BCY72	S3	Sm
BCY78	S3	Sm
BCY79	S3	Sm
BCY87	S3	Sm
BCY88	S3	Sm
BCY89	S3	Sm
BD131	S4a	P
BD132	S4a	P
BD135	S4a	P
BD136	S4a	P
BD137	S4a	P
BD138	S4a	P
BD139	S4a	P
BD140	S4a	P
BD201	S4a	P
BD202	S4a	P
BD203	S4a	P
BD204	S4a	P
BD226	S4a	P
BD227	S4a	P
BD228	S4a	P
BD229	S4a	P
BD230	S4a	P
BD231	S4a	P
BD233	S4a	P
BD234	S4a	P
BD235	S4a	P
BD236	S4a	P
BD237	S4a	P
BD238	S4a	P
BD239	S4a	P
BD239A	S4a	P
BD239B	S4a	P
BD239C	S4a	P
BD240	S4a	P
BD240A	S4a	P
BD240B	S4a	P
BD240C	S4a	P
BD241	S4a	P

* = series
FET = Field-effect transistors
Mm = Microminiature semiconductors for hybrid circuits
P = Low-frequency power transistors
Sm = Small-signal transistors

P = Low-frequency power transistors

P = Low-frequency power transistors
Sm = Small-signal transistors

FET = Field-effect transistors
HVP = High-voltage power transistors
Mm = Microminiature semiconductors for hybrid circuits
RFP = R.F. power transistors and modules
Sm = Small-signal transistors
WBT = Wideband hybrid IC transistors

* = series
FET = Field-effect transistors
Mm = Microminiature semiconductors for hybrid circuits
RFP = R.F. power transistors and modules
RT = Tripler
Sm = Small-signal transistors
ThM = Thyristor Modules
WBM = Wideband hybrid IC modules
WBT = Wideband hybrid IC transistors

type no.	book	section
BLV30/12	S6	RFP
BLV31	S6	RFP
BLV32F	S6	RFP
BLV33	S6	RFP
BLV33F	S6	RFP
BLV36	S6	RFP
BLV37	S6	RFP
BLV45/12	S6	RFP
BLV57	S6	RFP
BLV59	S6	RFP
BLV75/12	S6	RFP
BLV80/28	S6	RFP
BLV90	S6	RFP
BLV91	S6	RFP
BLV92	S6	RFP
BLV93	S6	RFP
BLV94	S6	RFP
BLV95	S6	RFP
BLV96	S6	RFP
BLV97	S6	RFP
BLV98	S6	RFP
BLV99	S6	RFP
BLW29	S6	RFP
BLW31	S6	RFP
BLW32	S6	RFP
BLW33	S6	RFP
BLW34	S6	RFP
BLW50F	S6	RFP
BLW60	S6	RFP
BLW60C	S6	RFP
BLW76	S6	RFP
BLW77	S6	RFP
BLW78	S6	RFP
BLW79	S6	RFP
BLW80	S6	RFP
BLW81	S6	RFP
BLW82	S6	RFP
BLW83	S6	RFP
BLW84	S6	RFP
BLW85	S6	RFP
BLW86	S6	RFP
BLW87	S6	RFP
BLW89	S6	RFP
BLW90	S6	RFP
BLW91	S6	RFP
BLW95	S6	RFP
BLW96	S6	RFP
BLW97	S6	RFP
BLW98	S6	RFP
BLW99	S6	RFP
BLX13	S6	RFP
BLX13C	S6	RFP
BLX14	S6	RFP
BLX15	S6	RFP
BLX39	S6	RFP
BLX65	S6	RFP
BLX65E	S6	RFP
BLX67	S6	RFP
BLX68	S6	RFP
BLX69A	S6	RFP
BLX91A	S6	RFP
BLX91CB	S6	RFP
BLX92A	S6	RFP
BLX93A	S6	RFP
BLX94A	S6	RFP
BLX94C	S6	RFP
BLX95	S6	RFP
BLX96	S6	RFP
BLX97	S6	RFP
BLX98	S6	RFP
BLY85	S6	RFP
BLY87A	S6	RFP
BLY87C	S6	RFP
BLY88A	S6	RFP
BLY88C	S6	RFP
BLY89A	S6	RFP
BLY89C	S6	RFP
BLY90	S6	RFP
BLY91A	S6	RFP
BLY91C	S6	RFP
BLY92A	S6	RFP
BLY92C	S6	RFP
BLY93A	S6	RFP
BLY93C	S6	RFP
BLY94	S6	RFP
BLY97	S6	RFP
BPF10	S8	PDT
BPF24	S8	PDT
BPW22A	S8	PDT
BPW50	S8	PDT
BPX25	S8	PDT
BPX29	S8	PDT
BPX40	S8	PDT
BPX41	S8	PDT
BPX42	S8	PDT
BPX71	S8	PDT
BPX72	S8	PDT
BPX95C	S8	PDT
BR100/03	S2	Th
BR101	S3	Sm
BRY39	S3	Sm
BRY56	S3	Sm
BRY61	S7	Mm
BRY62	S7	Mm
BSD10	S5	FET
BSD12	S5	FET
BSD20	S5	FET
BSD22	S5	FET
BSD212	S5	FET
BSD213	S5	FET
BSD214	S5	FET
BSD215	S5	FET
BSR12;R	S7	Mm
BSR13;R	S7	Mm
BSR14;R	S7	Mm
BSR15;R	S7	Mm
BSR16;R	S7	Mm
BSR17;R	S7	Mm
BSR17A;R	S7	Mm
BSR18;R	S7	Mm

FET = Field-effect transistors
Mm = Microminiature semiconductors for hybrid circuits
PDT = Photodiodes or transistors
RFP = R.F. power transistors and modules
Sm = Small-signal transistors
Th = Thyristors

INDEX

type no.	book	section	type no.	book	section	type no.	book	section
BSR18A;R	S7	Mm	BST76A	S5	FET	BTW40*	S2	Th
BSR30	S7	Mm	BST78	S5	FET	BTW42*	S2	Th
BSR31	S7	Mm	BSV15	S3	Sm	BTW43*	S2	Tri
BSR32	S7	Mm	BSV16	S3	Sm	BTW45*	S2	Th
BSR33	S7	Mm	BSV17	S3	Sm	BTW58*	S2	Th
BSR40	S7	Mm	BSV52;R	S7	Mm	BTW59*	S2	Th
BSR41	S7	Mm	BSV64	S3	Sm	BTW63*	S2	Th
BSR42	S7	Mm	BSV78	S5	FET	BTW92*	S2	Th
BSR43	S7	Mm	BSV79	S5	FET	BTX18*	S2	Th
BSR50	S3	Sm	BSV80	S5	FET	BTX94*	S2	Tri
BSR51	S3	Sm	BSV81	S5	FET	BTY79*	S2	Th
BSR52	S3	Sm	BSW66A	S3	Sm	BTY91*	S2	Th
BSR56	S7/S5	Mm/FET	BSW67A	S3	Sm	BU208A	S4b	SP
BSR57	S7/S5	Mm/FET	BSW68A	S3	Sm	BU208B	S4b	SP
BSR58	S7/S5	Mm/FET	BSX19	S3	Sm	BU326	S4b	SP
BSR60	S3	Sm	BSX20	S3	Sm	BU326A	S4b	SP
BSR61	S3	Sm	BSX45	S3	Sm	BU426	S4b	SP
BSR62	S3	Sm	BSX46	S3	Sm	BU426A	S4b	SP
BSS38	S3	Sm	BSX47	S3	Sm	BU433	S4b	SP
BSS50	S3	Sm	BSX59	S3	Sm	BU505	S4b	SP
BSS51	S3	Sm	BSX60	S3	Sm	BU508A	S4b	SP
BSS52	S3	Sm	BSX61	S3	Sm	BU705	S4b	SP
BSS60	S3	Sm	BSY95A	S3	Sm	BU806	S4b	SP
BSS61	S3	Sm	BT136*	S2	Tri	BU807	S4b	SP
BSS62	S3	Sm	BT137*	S2	Tri	BU824	S4b	SP
BSS63;R	S7	Mm	BT138*	S2	Tri	BU826	S4b	SP
BSS64;R	S7	Mm	BT139*	S2	Tri	BUS11;A	S4b	SP
BSS68	S3	Sm	BT149*	S2	Th	BUS12;A	S4b	SP
BSS83	S5	FET	BT151*	S2	Th	BUS13;A	S4b	SP
BST15	S7	Mm	BT152*	S2	Th	BUS14;A	S4b	SP
BST16	S7	Mm	BT153	S2	Th	BUT11;A	S4b	SP
BST50	S7	Mm	BT155*	S2	Th	BUV82	S4b	SP
BST51	S7	Mm	BT157*	S2	Th	BUV83	S4b	SP
BST52	S7	Mm	BTV24*	S2	Th	BUV89	S4b	SP
BST60	S7	Mm	BTV34*	S2	Tri	BUW11;A	S4b	SP
BST61	S7	Mm	BTV58*	S2	Th	BUW12;A	S4b	SP
BST62	S7	Mm	BTV59*	S2	Th	BUW13;A	S4b	SP
BST70A	S5	FET	BTV60*	S2	Th	BUW84	S4b	SP
BST72A	S5	FET	BTW23*	S2	Th	BUW85	S4b	SP
BST74A	S5	FET	BTW38*	S2	Th	BUX46;A	S4b	SP

* = series
FET = Field-effect transistors
Mm = Microminiature semiconductors for hybrid circuits
Sm = Small-signal transistors

SP = Low-frequency switching power transistors
Th = Thyristors
Tri = Triacs

* = series
PM = Power MOS transistors
R = Rectifier diodes
SP = Low-frequency switching power transistors

* = series
D = Displays
LED = Light-emitting diodes
Mm = Microminiature semiconductors for hybrid circuits
Ph = Photoconductive devices
PhC = Photocouplers
R = Rectifier diodes
TS = Transient suppressor diodes
Vrf = Voltage reference diodes
Vrg = Voltage regulator diodes

GD = Germanium diodes
I = Infrared devices
LED = Light-emitting diodes
P = Low-frequency power transistors
Ph = Photoconductive devices
R = Rectifier diodes
SD = Small-signal diodes
Sm = Small-signal transistors
St = Rectifier stacks
Vrf = Voltage reference diodes
WBM = Wideband hybrid IC modules

A = Accessories
I = Infrared devices
FET = Field-effect transistors
Ph = Photoconductive devices
R = Rectifier diodes
RFP = R.F. power transistors and modules
SD = Small-signal diodes
Sm = Small-signal transistors
WBT = Wideband hybrid IC transistors

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